Details are important
How can the designer help to make cleaning of assemblies easy

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ABSTRACT

This article shows some experiences from nearly 30 years of developing the PCB cleaning process, building cleaning machines for defluxing, and helping hundreds of companies optimize cleaning technology.

The main Challenge of Cleaning Electronic Assemblies.

Cleaning electronic assemblies to be "nice" (shiny) on it´s open surface easy. Even a simple, cheap machine (dishwasher) may serve well for such tasks.

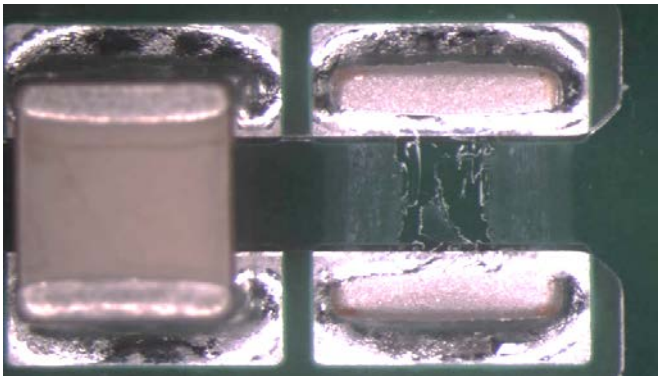


Figure 1: Incompletely cleaned gap. The light areas are ionic active residues

Such a simple process cannot clean entirely under the gap. However, by such uncomplete cleaning, we substantially damage the assembly's quality. Residues, which are not thoroughly cleaned, have an open structure and active ionic compounds exposed. These cause ion migration.

The effect of uncomplete cleaning is visible on the SIR test record from the PCB B-52- Legacy 2

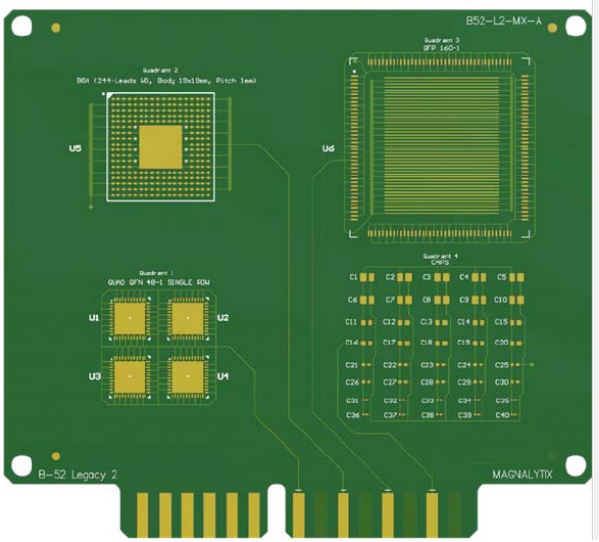


Figure 2: SIR test board B-52 Legacy 2 PD [3]

The results of the SIR test are on the following graph. The QFN and QFP were not thoroughly cleaned.

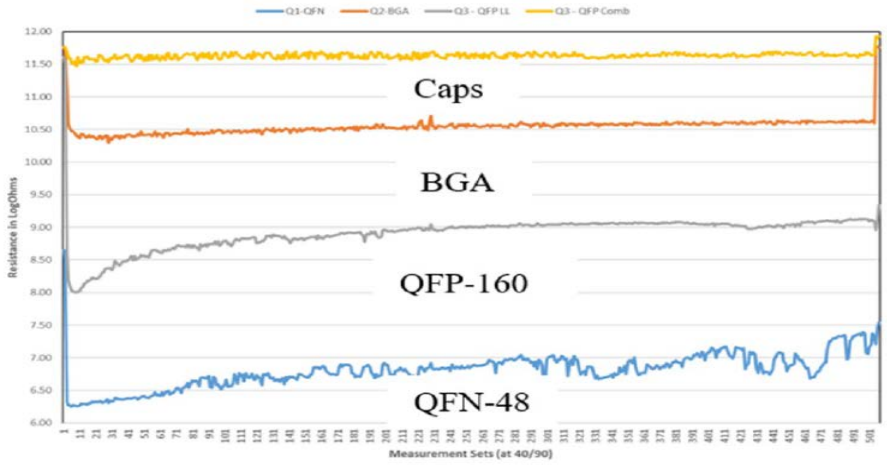


Figure 3: SIR test record of B52 Legacy 2 incompletely cleaned. The QFN48 shows unacceptable resistance, and the QFP-160 resistance is at the limit of acceptability [2]

How big is the Standard Gap?

The gap thickness is a play between the thickness of the pad on PCB, solder mask thickness, and solder thickness.

The Thickness of the Solder

A typical thickness is about 50-60% of the printed thickness. So, by a typical print thickness of 120um, we get about 60um primary solder thickness.

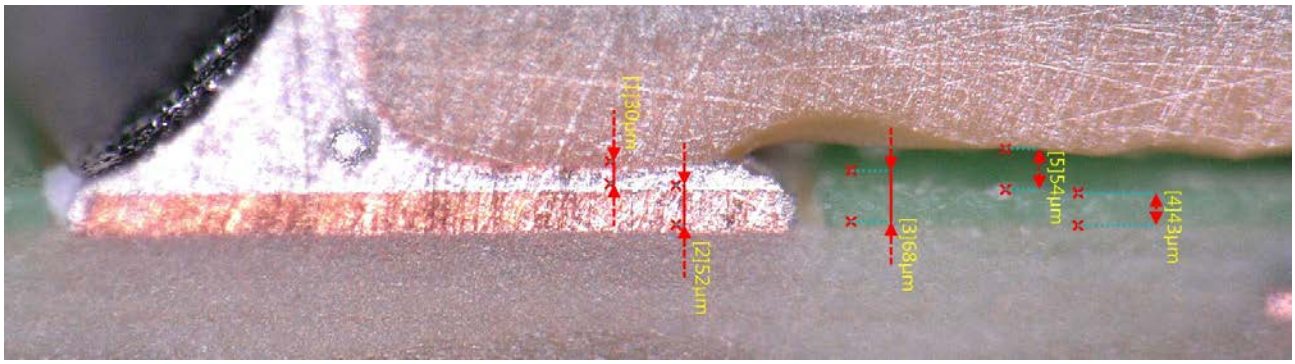


Figure 4: standard and reasonable proportion of gap under MLCC

However, the actual thickness depends also on the mass of the component. More precisely, it depends on the "draft" of the components.

During soldering, the component is swimming on the liquid solder.

The Thickness of the Solder Mask and Pad

The thickness of the solder mask must be no bigger than the thickness of the pad. The thinner the solder mask- the better!

Due to the optimal solder paste printing process, a solder paste thickness equal to pad height is recommended.

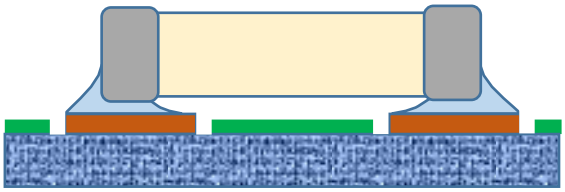


Figure 5: Solder mask thinner than the pad – easy cleanable

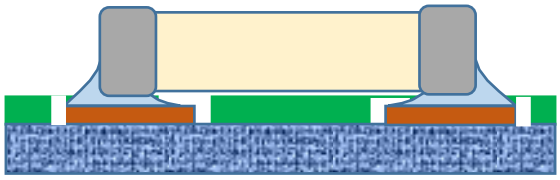


Figure 6: Solder mask thicker than the pad – challenging to clean

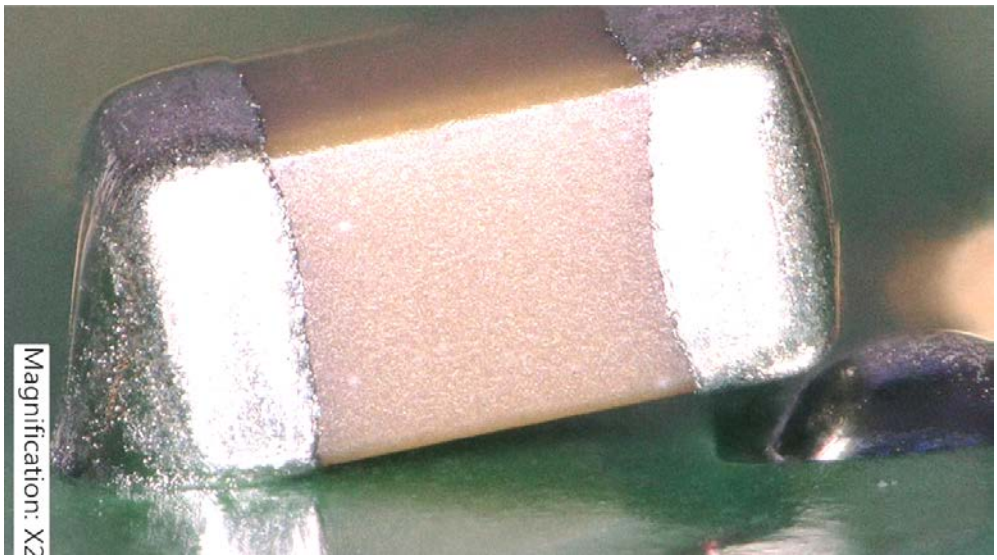


Figure 7: A tombstone caused by too thick solder mask.

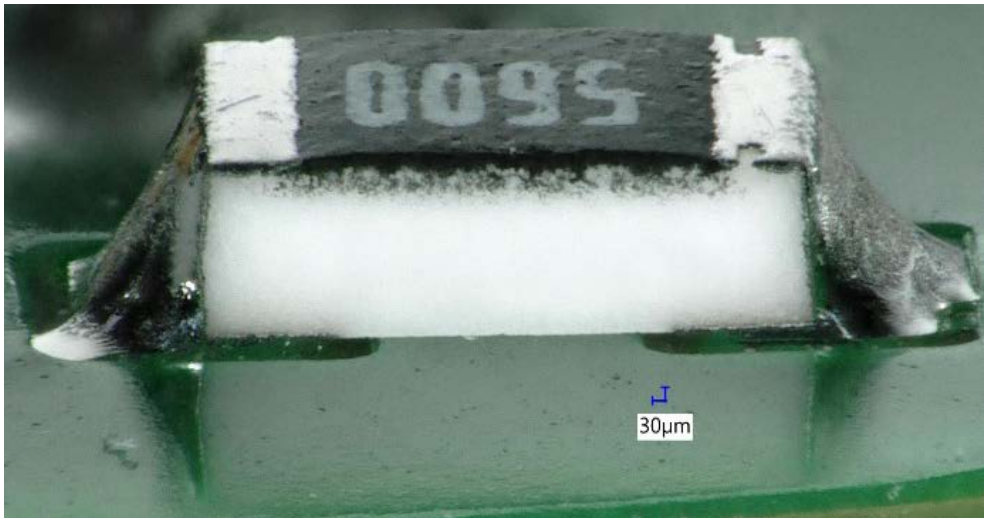


Figure 8: Gap = 0, due to too thick solder mask!

COMPONENTS WITH AN EXTREMELY THIN GAP

Cylindrical Body Components MELFs

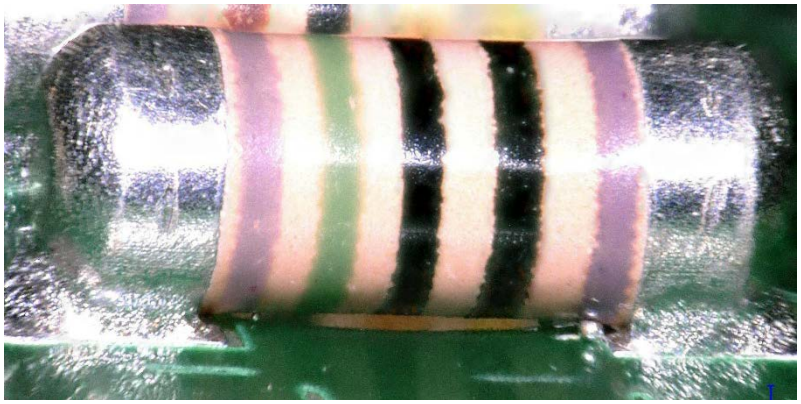


Figure 9: Residues under MELF – the gap goes to 0. Mention uncleaned flux residues under the component body (this is not an SMT glue!)

Unstable Component Body

Some packages like SOD123FL have too narrow terminals and a high gravity point, so they tend to tilt during soldering.

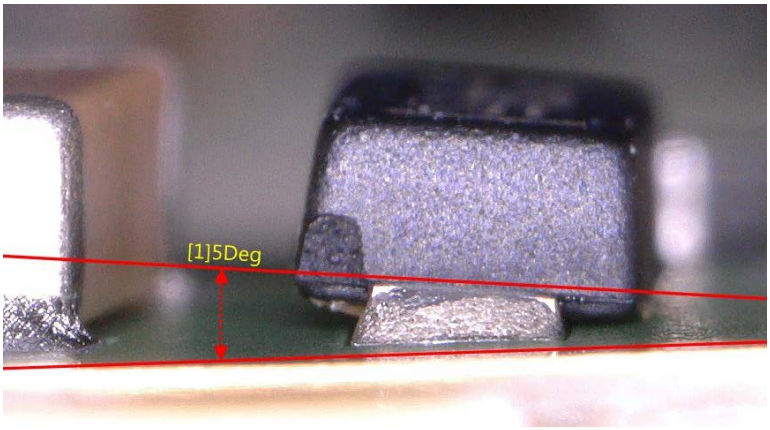


Figure 10: tilted SOD123FL package

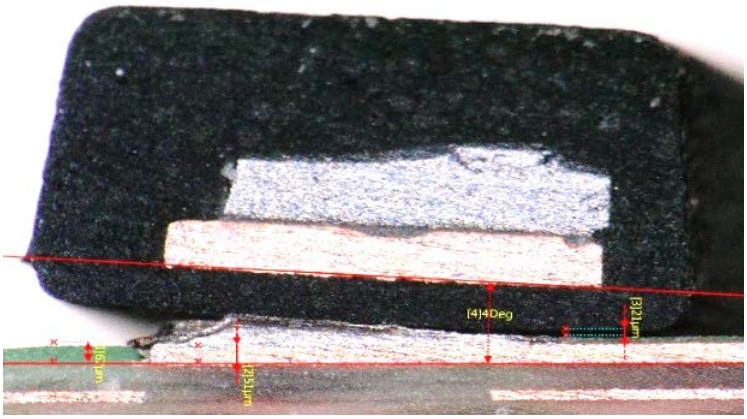


Figure 11: cross-section of tilted SOD. Mention the package sitting closely on the solder mask of the side connection of the pad.

Figure 12: Typical residue pattern after cleaning of tilted SOD

Local reductions of the gap.

Cleaning under the thin gap requires no obstacles for cleaning liquid flow. Even in most CAD design rules, the line under the chip is a common element. However, we should not use such a feature for perfect cleaning under components at highly reliable boards!

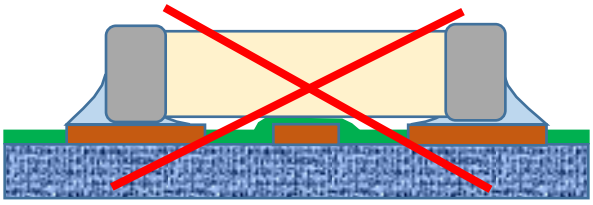


Figure 13: Line under chip closes the gap

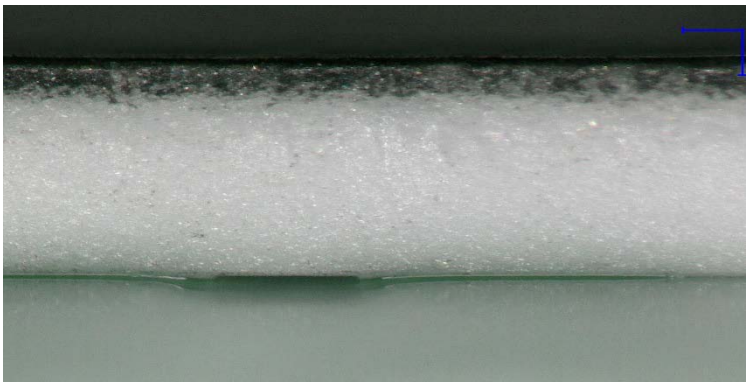
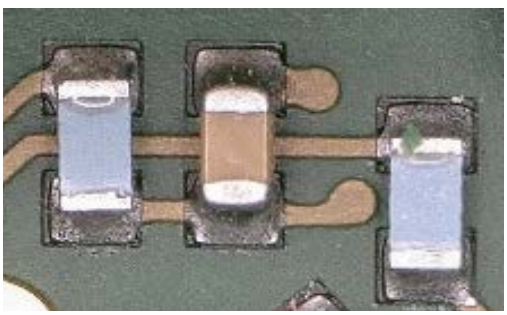


Figure 14: total reduction of gap due to two broad line areas under the chip

The line positioning under the chip components is a frequent design failure. It does not matter under components with leaded terminals (PLCC, QFP, SOIC) with a gap size higher than 100um. Still, for any chip and bottom terminated component to be cleaned, it causes challenges.



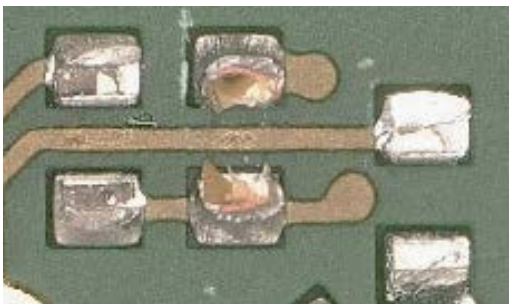


Figure 15: Line under chip – thoroughly cleaning takes 50min. Cleaning the gap under the similar chip w/o line takes y 20min only.

Pad Outline shall copy the Component Terminal Outline.

Suppose the component has a heat dissipating area on its lower side. In that case, the same should be on the PCB (even if it is not necessary due to low heat dissipation!).

If there is no pad on the PCB opposite the heat dissipator, the solder wicks along the thermal dissipator and closes the gap.

Figure 16: SOT223 and residues under the body after tearing.

Between the package's solder mask and thermal pad, a thin continuous layer of flux residues forms in such case. This hardly cleanable area can also affect neighboring terminals and cause current leakages. Such flux residues are visible on the SOT223 package after tearing (see Figure 18)

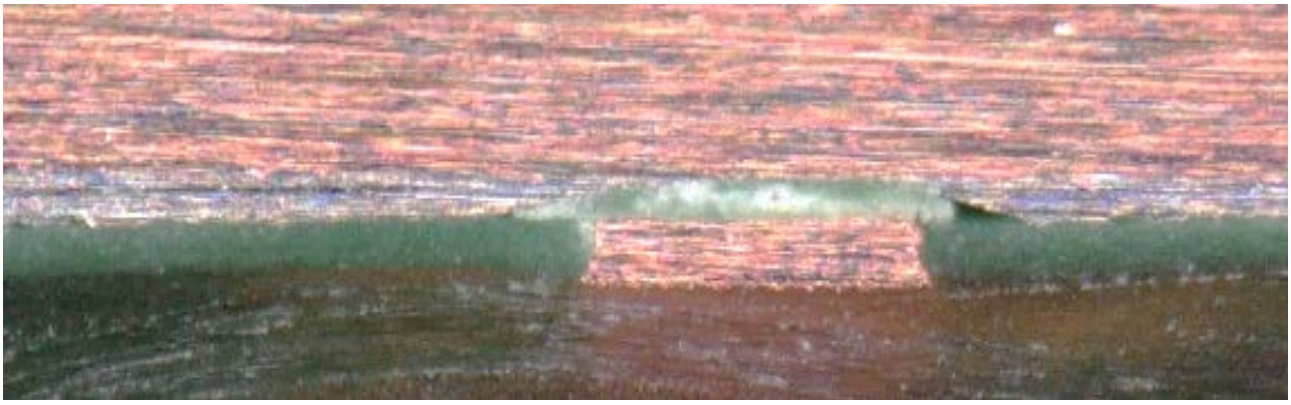
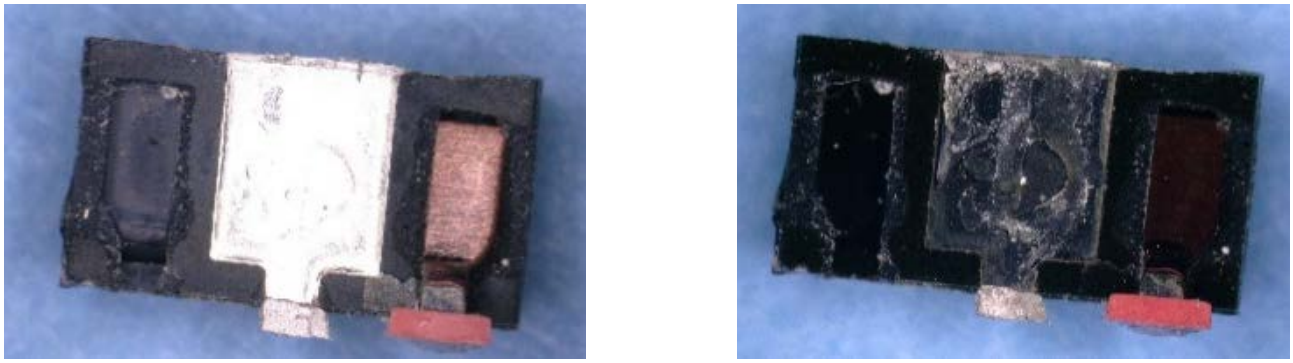


Figure 17: cross-section of the soldered SOT223. The heat dissipater on the package wicks solder. The solder closes the gap under the component. Between the mask and solder uncleanable is an uncleanable flux residue.



F**igure 18:** picture of SOT223 after tearing. Flux residues are only visible in polarized light (right picture).

Obstacles on the Packages

A typical example is a tantalum capacitor package. This package has a protrusion on the bottom side. It should help the component body to reach the droplet of glue. For assembly mounted with solder paste which should be cleaned, it interferes with the cleaning. Such a relict comes from the early age of SMT when most SMT components were glued.

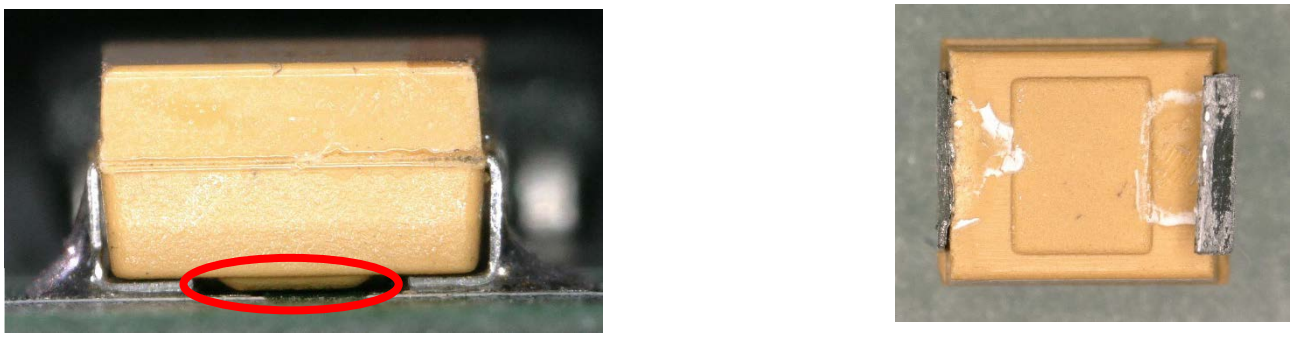


Figure 19: protrusion for glue on the tantalum capacitor package.

Reverse Format Chips

Components with long terminals and narrow bodies (resistors, capacitors) are suitable for transmitting high power. Long terminals can easier dissipate higher energy losses. Such components, however, cause a kind of cleaning challenge. Cleaning time must be longer.

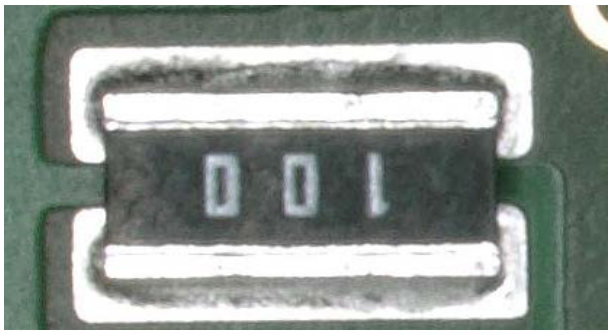


Figure 20: Reverse format resistor

We compared the cleaning of two models on the Glass Test Board – 0805 size and 1108 size (about the double-length, the same width). For the same cleaning conditions, the cleaning time to complete cleaning is about three times longer for two times longer channel under the chip.

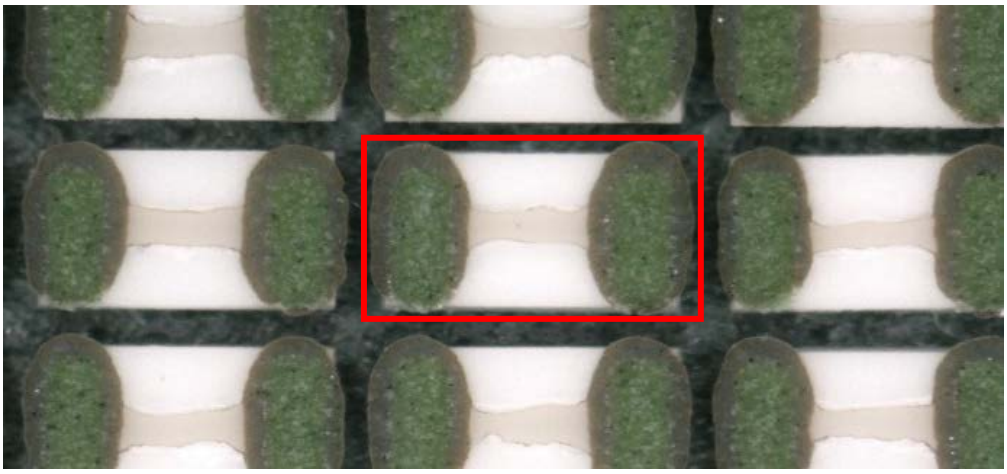


Figure 21: Glass Test Board GTB400 with chip models 0805 sizes, partially cleaned

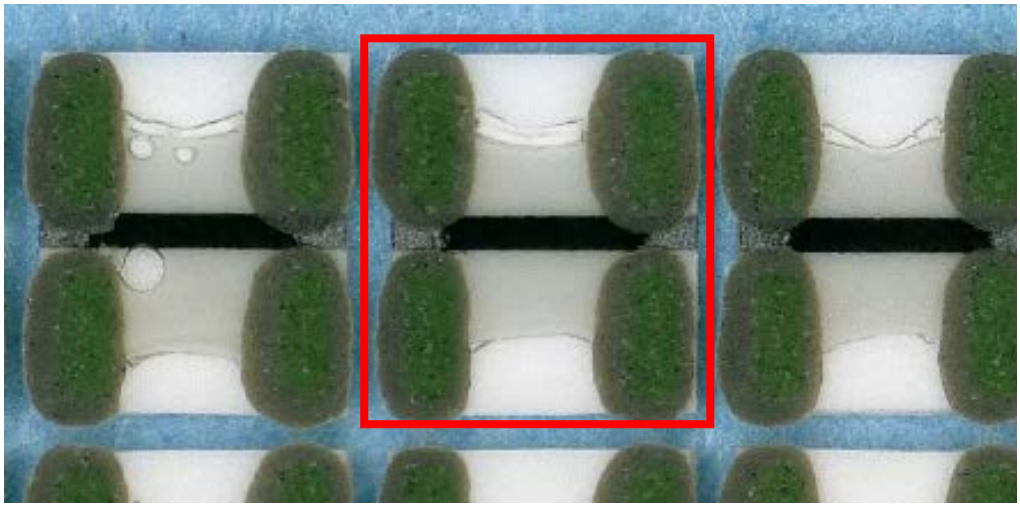


Figure 22: Glass Test Board GTB200 with chip models 1108 sizes, partially cleaned

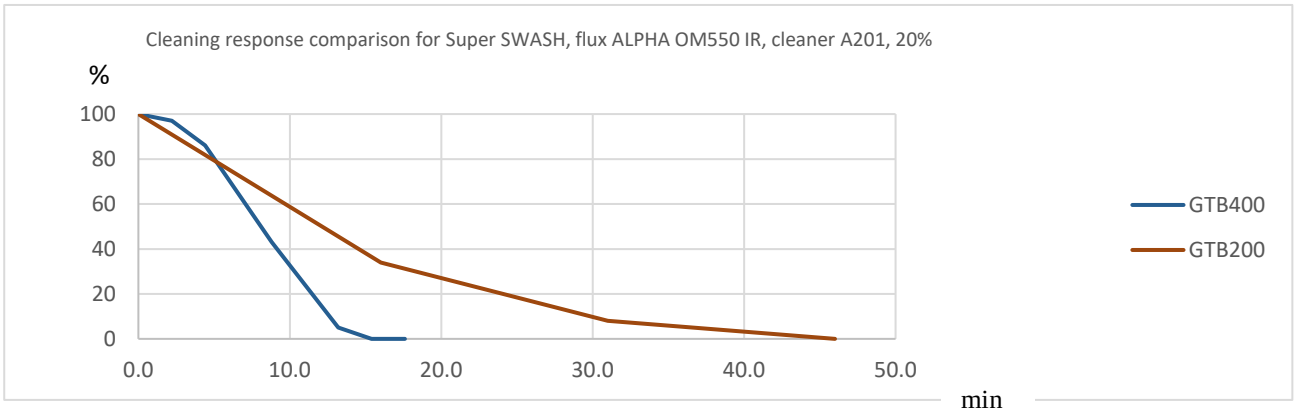


Figure 23: Cleaning response comparison of Glass Test Board with 0805 and 1108 chips.

Chips with reverse geometry are more sensitive to the shadowing effects by other components. Such geometry causes an enormous increase in cleaning time to manage such challenges.

Designing a row of reverse geometry chips terminated by another component with a low gap (for example, a tantalum capacitor at the end of the row) may be critical.

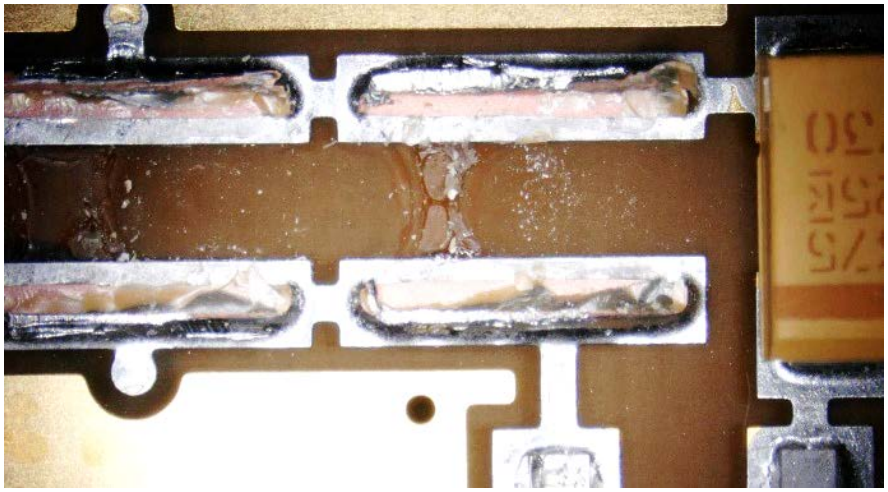


Figure 24: Row of reverse geometry chips with shadowing components at one end of the row.

Additionally, a combination of reverse geometry and difficult–to–clean flux residues may be critical. Figure xx shows flux residues from jet-printed solder paste. The assembly is w/o solder mask – gap under a chip, in this case, is 70-80um. (see Figure 24)

The combination of reverse geometry with the line between terminals is critical for cleaning, even if the flux/ cleaner combination is optimal

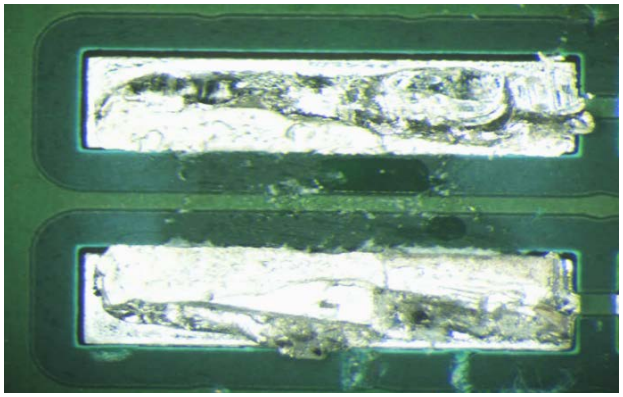


Figure 25: The reverse geometry chip and line under component on the assembly with solder mask.

Large area gaps

Typical examples (and often design failures) are daughter boards mounted directly parallel to the motherboard. The daughterboard is usually much larger than the standard component package, and liquid loses energy to dissolve residues deep in the gap. Even the distance between both boards is relatively high (100-200ųm).

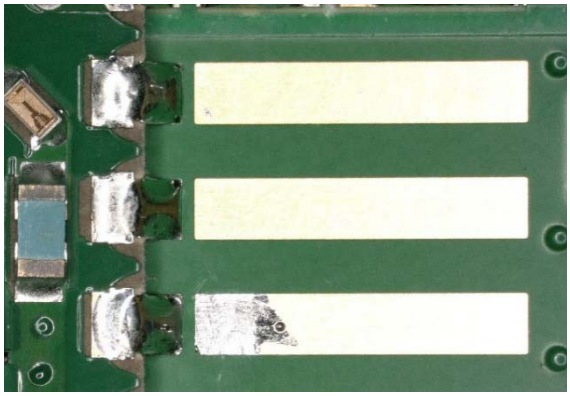


Figure 26: Daughterboard soldered directly on the motherboard

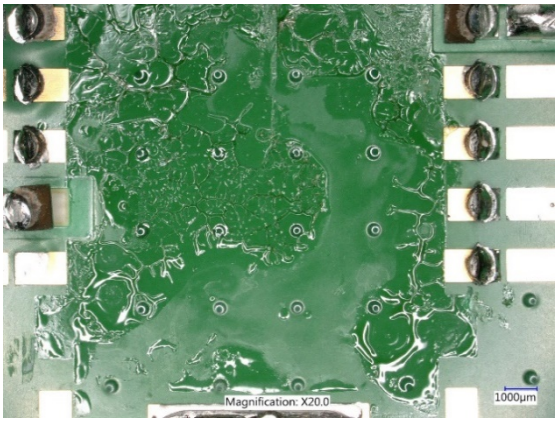


Figure 27: Residues after cleaning under the daughterboard (gap <100um, board size 13x13mm)

Lifting the daughterboard to 0,5-1mm will help substantially. (Flattened posts may be a good option)

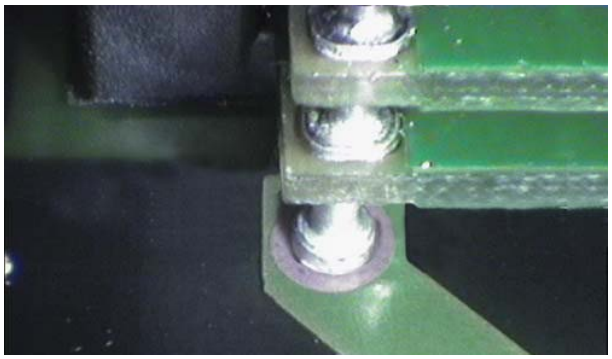


Figure 28: parallel boards soldered through flattened posts

Leaded SMT Components

Leaded SMT components are generally easy to clean. Due to the terminal design, their body distance from the PCB is higher than 100ųm.

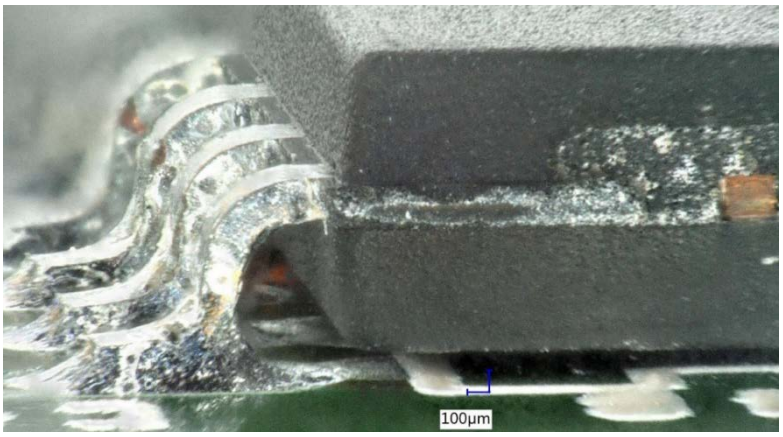


Figure 29: Cleaning under SOIC with a gap height of 150um is easy.

The only challenge is caused by a shifted solder mask image against the solder pad image. Then leads are very close to the pad aperture of the solder mask.

Figure 30: Shifted solder mask pattern with minor residues between lead and edge of solder mask

Usually, with an optimal cleaner choice for the flux residues, even such a narrow space can be cleaned.

Bottom terminated Components - BGA

Flux residues rarely fill the BGA or CSP gap. Therefore, cleaning is easier from the beginning. (Unless the pin count goes not over 2000 with ball size less than 0,5mm, or the gap is filled with flux – which may happen by BGA's with the central heat dissipating area.) Today, BGA does not represent a particular cleaning challenge.

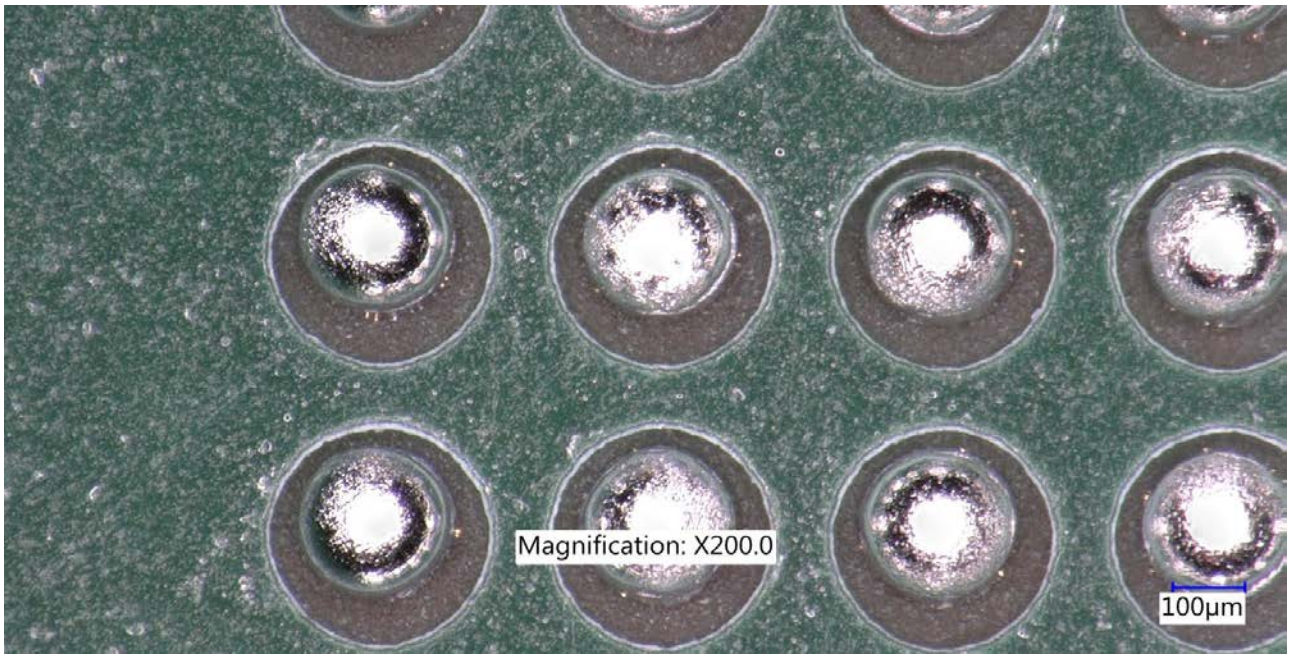


Figure 31: Cleaned gap under the flip-chip package, Ball size 150um, Silicon chip sheared- off down.

Challenges in BGA Cleaning - central BGA area without Terminals

The central area of BGA without balls usually does not have many flux residues. However, cleaning flux residues from here is problematic. Cleaning liquid loses kinetic energy by turbulences behind balls in the rows.

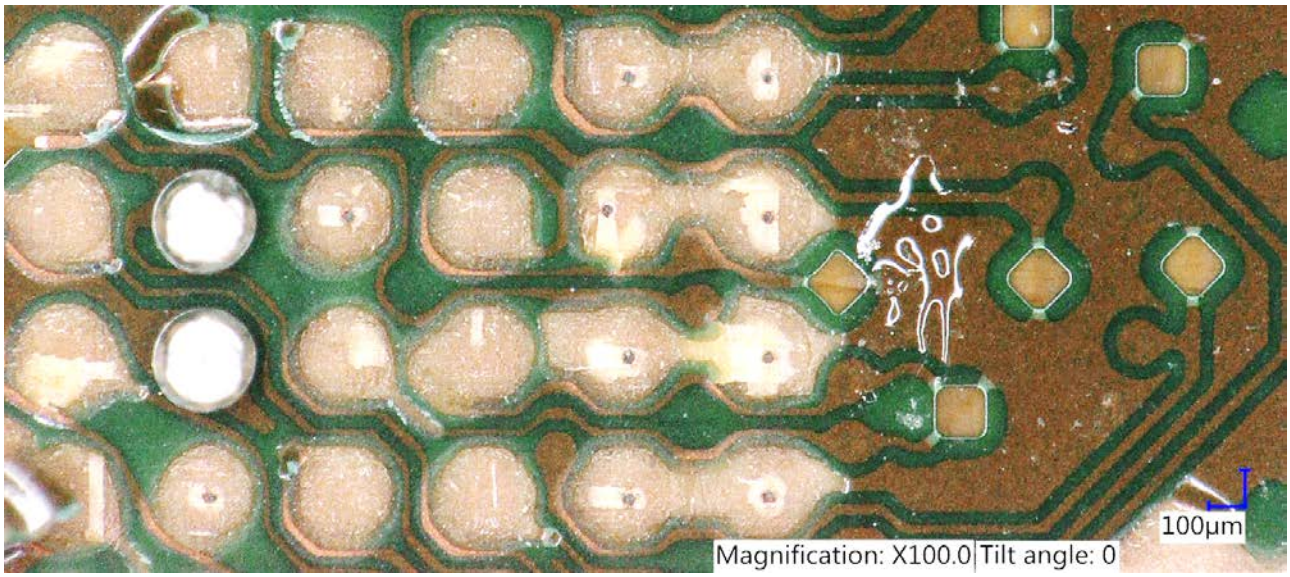


Figure 32: Part of BGA after cleaning with flux residues in the central area.

Designers often use the free central BGA area to position capacitors, especially for high-frequency applications. However, for applications requiring cleaning, such a design is not suitable. Thorough cleaning in a thin gap under the capacitor positioned under BGA requires a good combination of cleaner and residues and an extremely long cleaning time.

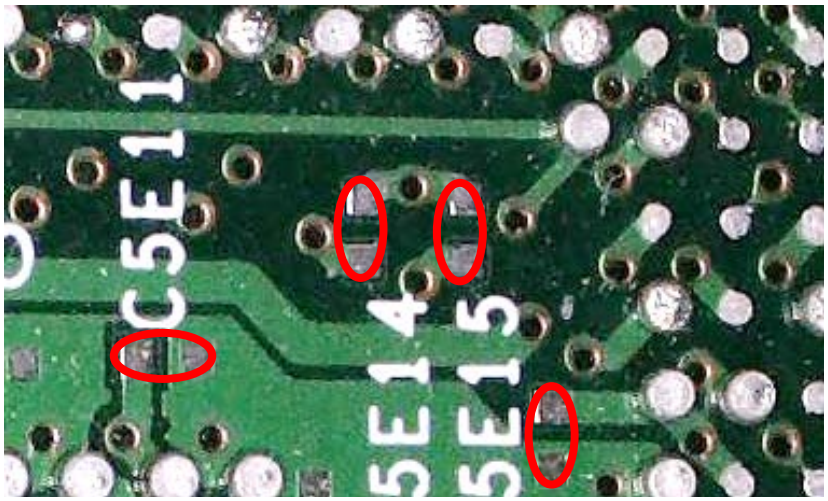


Figure 33: shows well-cleaned capacitors gaps under the BGA (particles generated by tearing off the BGA)

Solder Mask Configuration - Influence on BGA Cleaning

The cleaning of BGA can be simplified by designing a suitable solder mask configuration. There are generally,

three possibilities:

- Standard solder mask (SM- with some gap between pad and mask),
- Non-solder mask (NSM- omitted solder mask between pads),
- Solder mask defined pad (SMDP- solder mask covers a periphery of the solder pad.)

Our experience says the SMDP is the best option, especially for BGA and CSP, with minimal ball diameter and terminal pitch.

Covering the pad periphery makes the wettable pad area smaller. This results in lifting the component, thus better outgassing during soldering and better cleaning ability. Also, the gap size increases. Some overprint of solder paste over the solder mask is not critical (current solder paste fluxes are much better than in the past.)

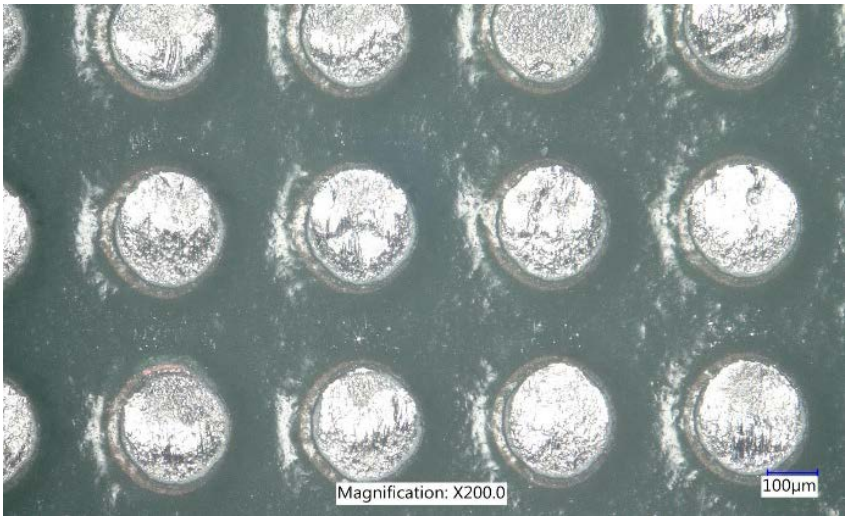


Figure 34: BGA with SMDP – pitch 300um, gap height 150um, washing time 2 min.

Bottom terminated Components

Components with terminals only on the bottom side of the package are currently the biggest challenge for cleaning. The main reason is a very tiny gap of 40-20um. The gap is always fully filled with flux residues. Because of a critical balance between pad height and resulting gap, the design of QFN uses mainly an NSM.

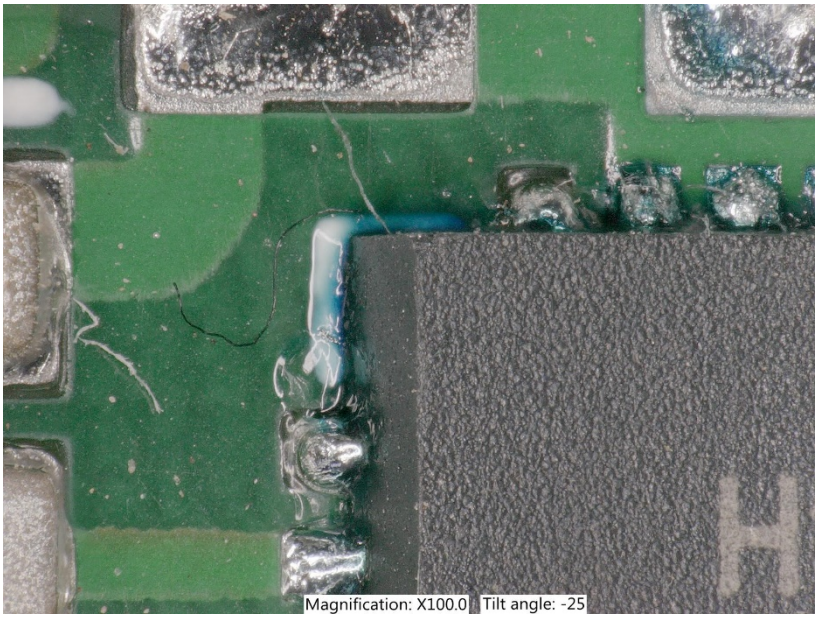


Figure 35: QFN before cleaning

Figure 36: the same QFN after cleaning

Flux residues under BTC components after soldering usually contain more vehicles and activators. They cannot oxidize and boil out from the flux during soldering in the large, closed gap. It is challenging to reach high surface resistance and reliability in such a situation. The study [2] shows that the gap size influences surface resistance. The gap size with Non-Solder Mask (NSM) is about twice big as with Solder mask Defined pads (SMDP)! Outgassing at NSM is much easier. Thus, a NO clean process must be thoroughly qualified for bottom terminated components.

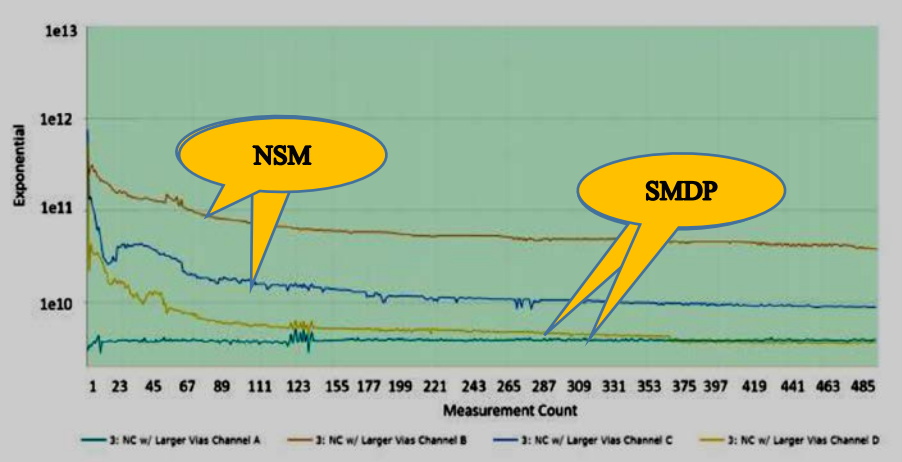


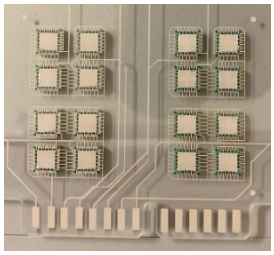
Figure 37: uncleaned QFN with different solder mask design [2] Non Solder Mask has better values of SIR

Cleaning is an essential option if we use BTC in highly reliable assemblies.

Precise diagnostics of cleaning results under the BTC components is almost impossible. Any attempt to remove such components after soldering is challenging due to the large soldered thermal dissipative area.

A good approach is using glass models, which can be evaluated optically and at the same time measured for the surface insulation resistance. [2]

Uncomplete cleaning results in leakage currents and dendrite growth between poles. It can be nicely visible in the following pictures made on unique Glass test boards



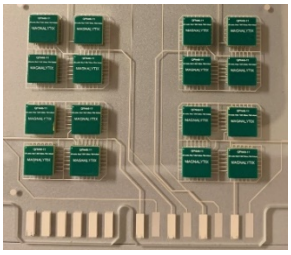


Figure 38: glass test board for SIR test with QFN component models (bottom and top-side)

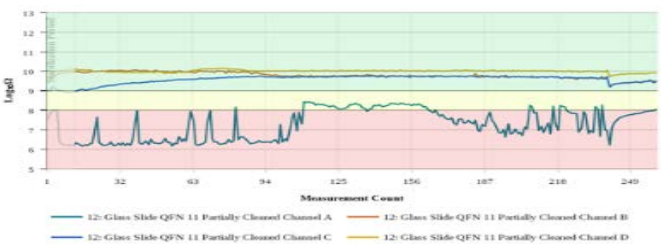


Figure 39: leakage currents on SIR test record and the detailed picture of the same component [2]

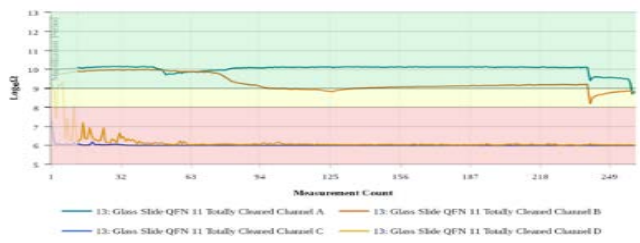


Figure 40: shorts and dendrite structure on the detail of the component [2]

RF Shieldings

Shieldings are always some obstacle to spray technology. Good design can minimize the cleaning time needed for the structure under the shielding. Suppose there is not an optimal design of the shielding. The cover shall have at least two well-dimensioned openings – one on the upper side one on the lowest point. Especial care must be taken for checking the effectivity of wash and rinsing in such a situation.

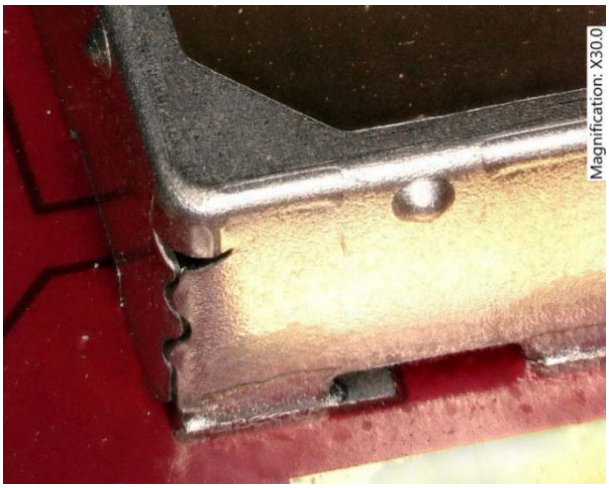


Figure 49: RF shielding for cleaning – the lid is clicked – on at the very end of the assembly process

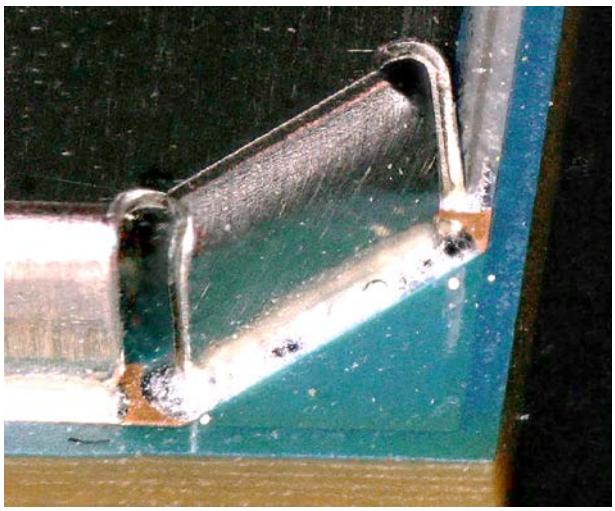


Figure 50: RF shielding with openings – Conditionally cleanable.

Open Components

The majority of the open components shall be delivered with seal labels or plugs to stop liquid penetration inside the component. Some open components (like membrane switches) could be cleaned as unsealed. Still, exceptional care must be put to proper rinsing. The rinsing result shall be checked regularly in QPM (quality process management system).

Cable, Cable Sleeves

Strands of the wire tend to wick the cleaner under insolation. It is reasonable to block wicking of cleaner as much as possible. Subsequent water rinsing may not be able to rinse cleaner from the strand wire. An adequately soldered end of the wire can help.

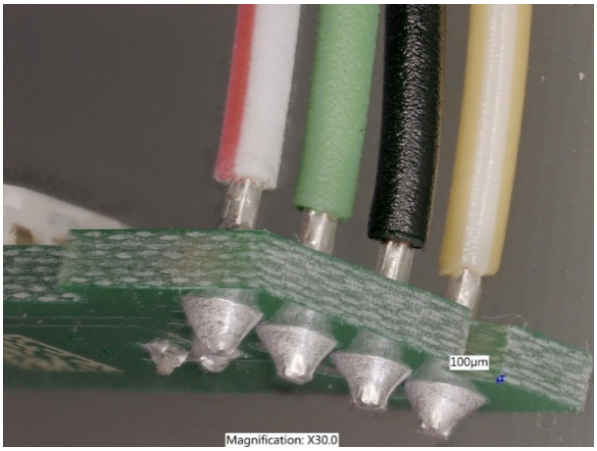


Figure 51: Properly soldered strand wires. Solder wicks under insulation but not too far to limit the flexibility. (also refer to the IPC 610 6.5.3)

Sleeves over the end of wire (at connectors or terminals) must be left unshrink before cleaning.

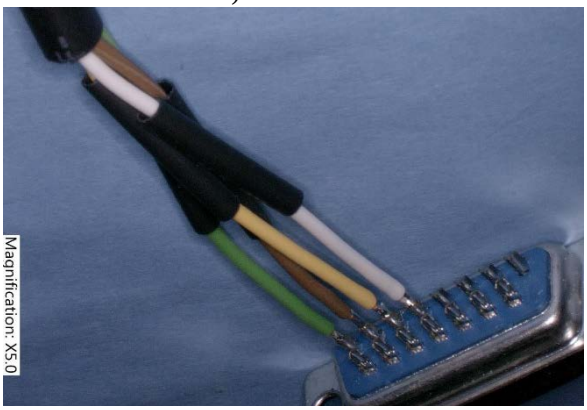


Figure 52: connector and cable before cleaning.

Figure 53: connector and cable after cleaning and shrinking

Conclusion

Electronic assemblies became to be more complex than in the past. The complexity and requirements for reliability and signal integrity moved the cleaning of electronic assemblies far from simple operation to complex technology. Designers can help reduce the cost of cleaning and, in many cases, even make the assembly cleanable. Knowledge of cleaning challenges may help to optimize the design. This concerns the design of assemblies and, unfortunately, in many cases, the design of packages.

Literature:

[1] Test reports of different cleaning trials (PBT Works, 2010 – 2022)

[2] Mike Bixenmann, Mark Mc Mean, Vladimír Sítko: (Conference APEX 2021 – professional development course, March 2021) – Design Reliable Electronics in accordance with IPCJ- STD-001H Section 8 Cleanliness

[3] Mike Bixenmann, Dough Pauls, Mark Mc Mean (Professional Development Course: Qualifying and controlling Clean and No- clean processes, APEX 2022