HYPERBITS™

Connector Design and Qualification for High Reliability CPCI SERIAL SPACE Applications

Presented by:

Gaby Cristian Mindreci - Performance Interconnect SAS

Dimas Morilla - ALTER TECHNOLOGY

PERFORMANCE INTERCONNECT

MINDREACH

ALTER TECHNOLOGY

1 Background

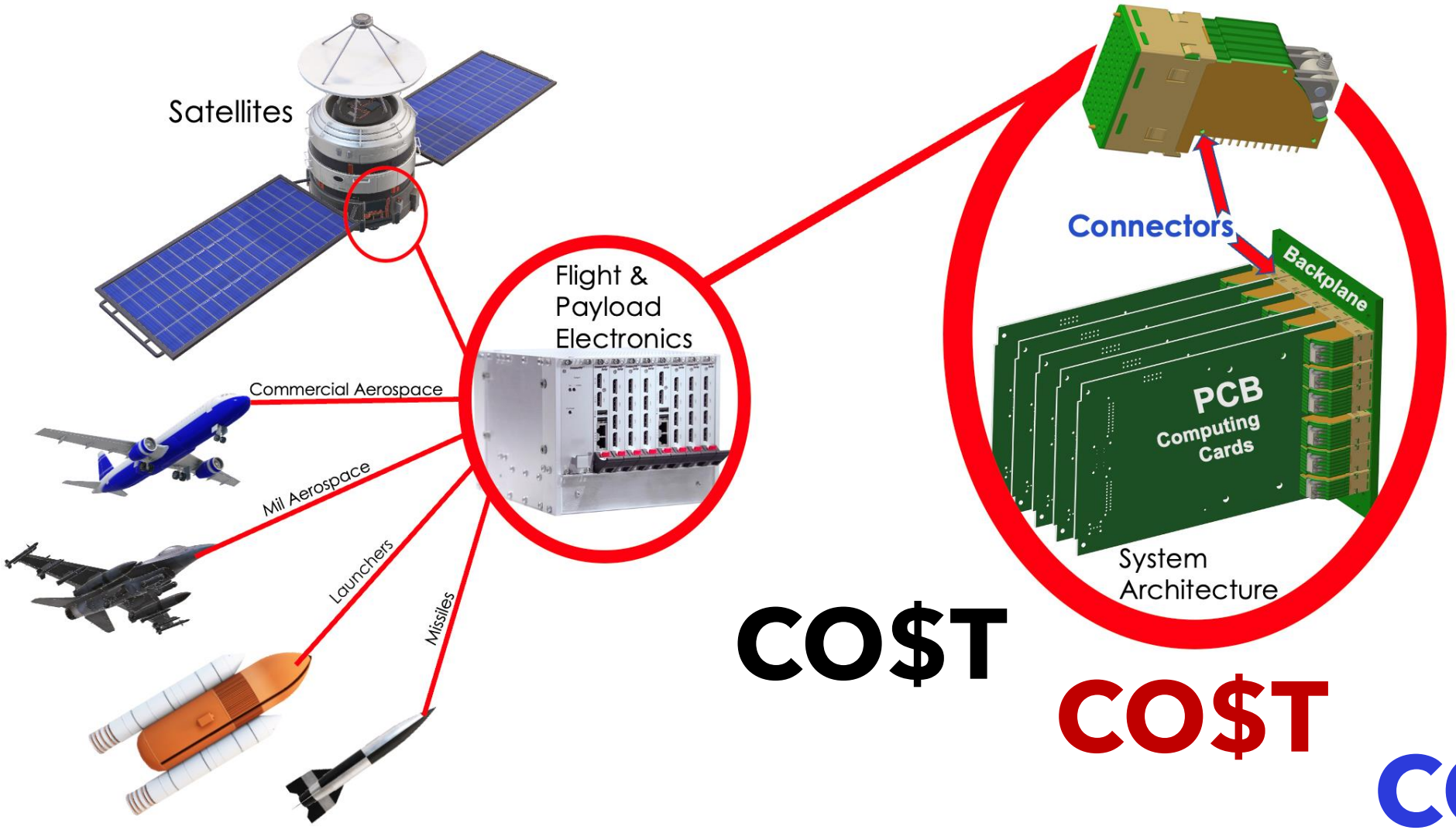
2 Solution

3 Specification

4 Test Plan

5 Conclusion

Where does it go and why choose cPCI Serial and not open VPX?



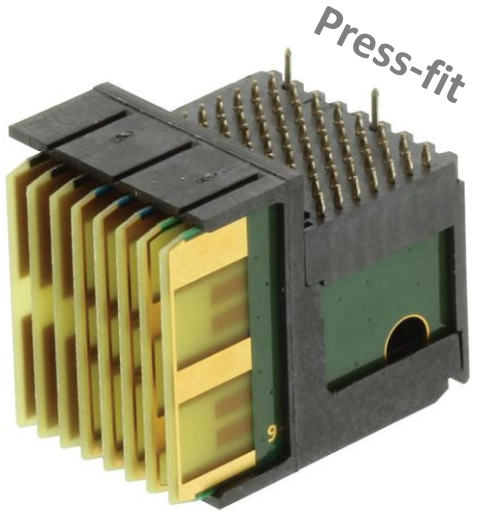
Connectors in cPCI Serial and open VPX

$ << $

Commercial

Amphenol

AIRMAX VS



Commercial/MIL

TE Connectivity

MULTIGIG RT

…but how about technical CHALLENGES?

From page 18 of:

CompactPCI® Connectors In Space Flight Applications

Prepared By:
Richard Williams (Code 562)
Kusum Sahu (Code 562)

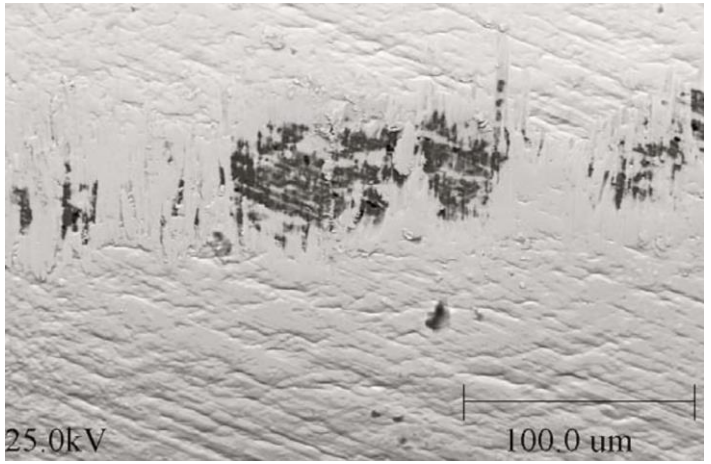
Reviewed By:
Dr. Henning Leidecker, (Code 562) Terry King (Code 562)
Dr. John Day (Code 560) AETD cPCI Review Committee

August 3, 2007

V. Reliability Issues and Mitigation Strategies Employed by NASA Space Flight Hardware Builders

"The two-point contact construction strategy employed in CompactPCI® connectors, coupled with the lack of a clamping mechanism to hold the mated pair together, leads to the intermittent loss of connectivity during vibration. Furthermore, fretting of the plating materials due to the relative movement of the blade shaped pins and bifurcated socket tines leads to an increase in contact resistance. Increased contact resistance directly correlates to a decrease in the quality of the electrical connection. "

''Cross-Section of CompactPCI® Bifurcated Socket Tines (Diane Kolos, NASA/GFSC). Magnification is 8x.''



'' Example of Fretting as reported in Ball Aerospace DPA following vibration testing. Darkened region is exposed base metal.''

Recent TIMELINE related to **cPCI Serial Space connector** developments:

1 **AUG 2017**

PICMG released
cPCI Serial Space
Specification
CPCI-S.1 R1.0

2 during **2020**

ADHA
Advanced Data Handling Architecture
consortium
formed by
ADS, TAS & **Ruag**

3 **MAR 2021**

ADS
releases specification for
cPCI Serial Space
Connector
Ref: DOC-EEE-000218505

4 **SEPT 2021**

MIND REACH

files IP protection for Single-Piece
High Data Rate
Backplane Connector
HYPERBITS™

5 **MAR 2022**

MIND REACH &
ALTER TECHNOLOGY
enter in collaboration agreement
to validate and qualify HYPERBITS™
to ESCC 3401 and CPCI-S.1 R1.0

6 **APR 2022**

ESA releases
RFP for Procurement and Reliability
Assessment of High Data Rate
Press-Fit cPCI SS connectors

7 **JUL 2022**

ESA Tender Action
is released under **ARTES**
for development of space qualified
high-density electrical
interconnections
for CPCI-S.1 R1.0

8 **AUG 2022**

MIND REACH
awards license for
S-FECT™ Technology & **HYPERBITS™** to
PERFORMANCE INTERCONNECT

9 **DEC 2022**

ALTER TECHNOLOGY
shall commence evaluation activities
of CPCI Serial commercial
connectors and
HYPERBITS™ connectors

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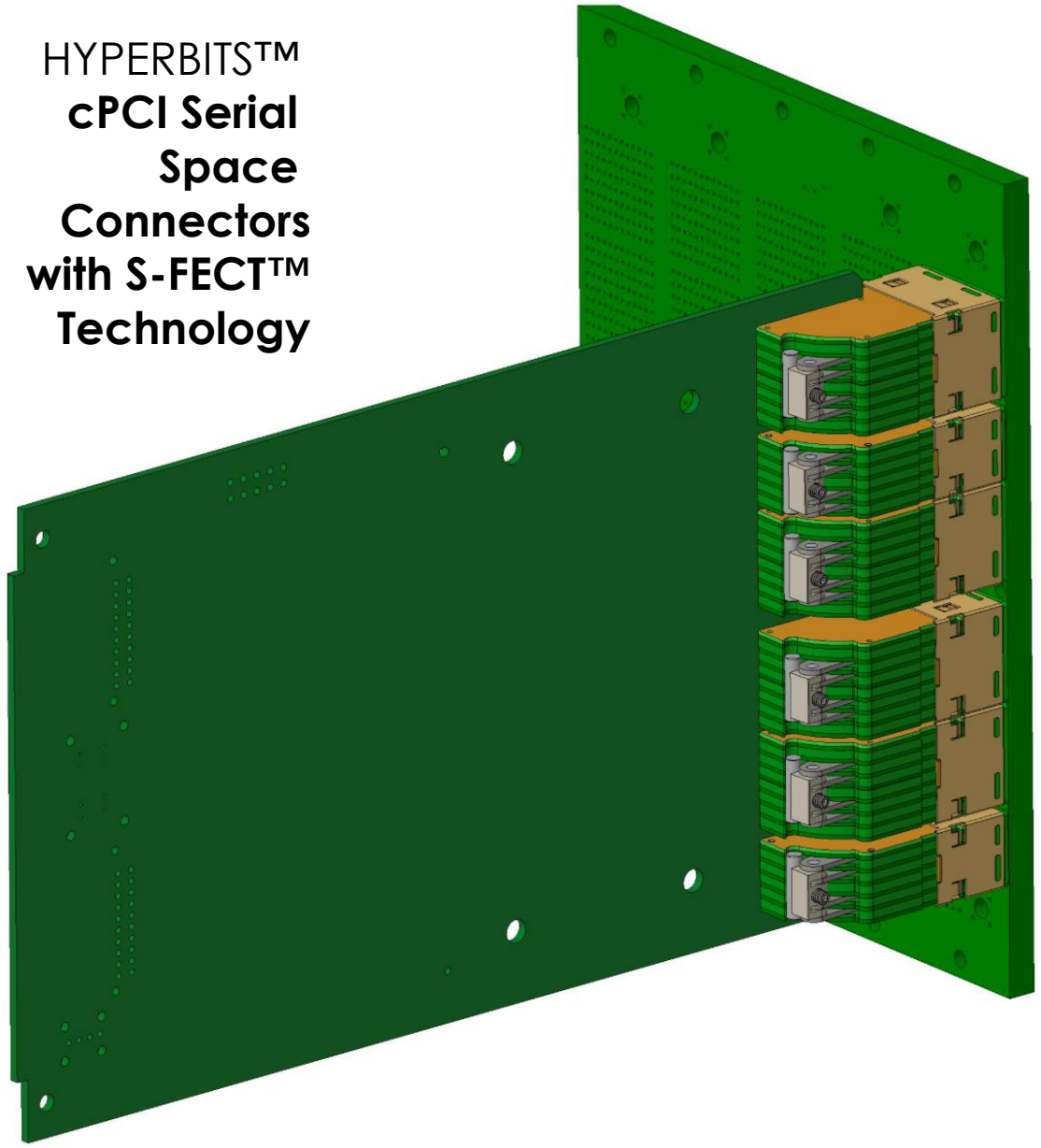
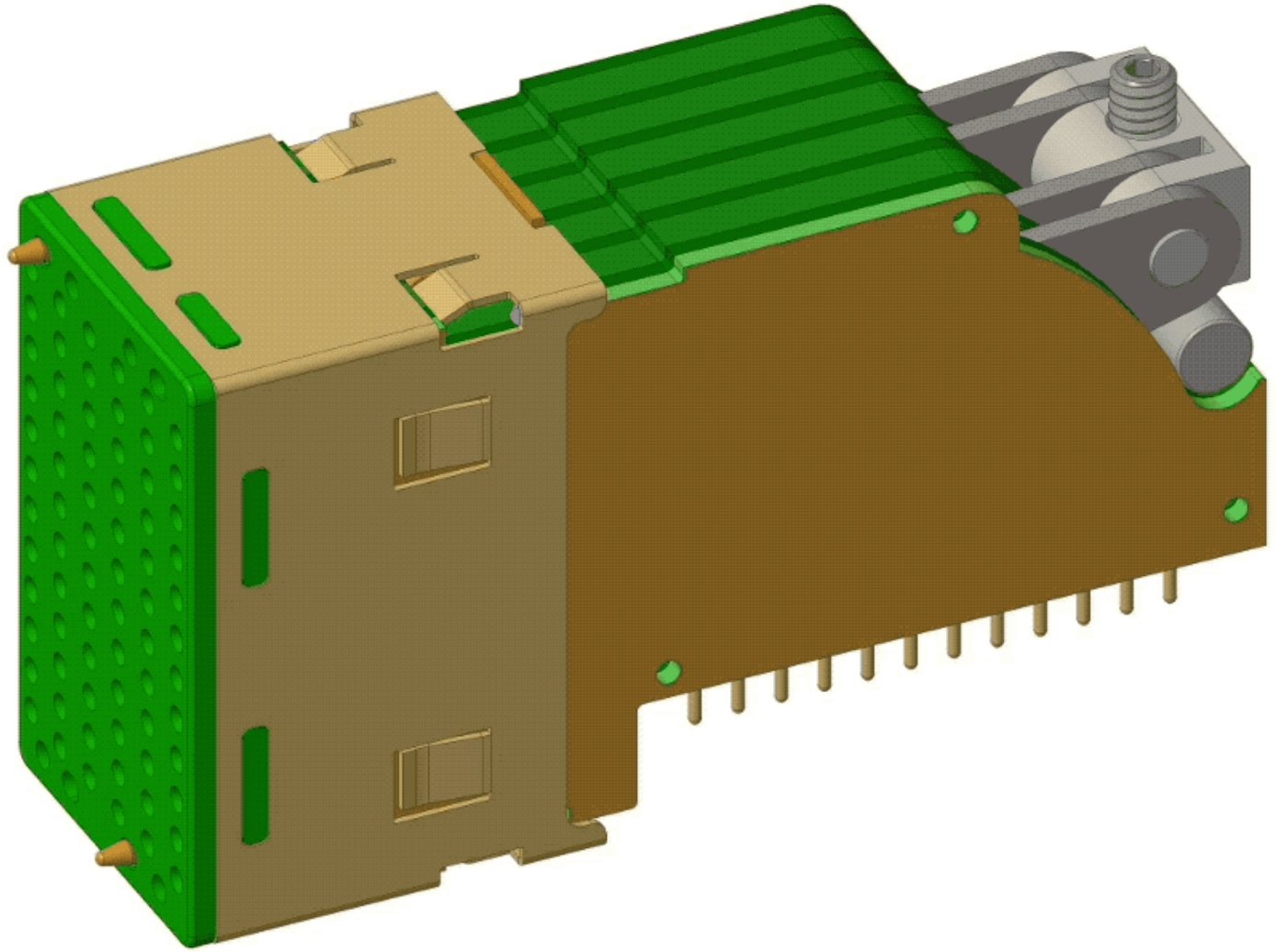
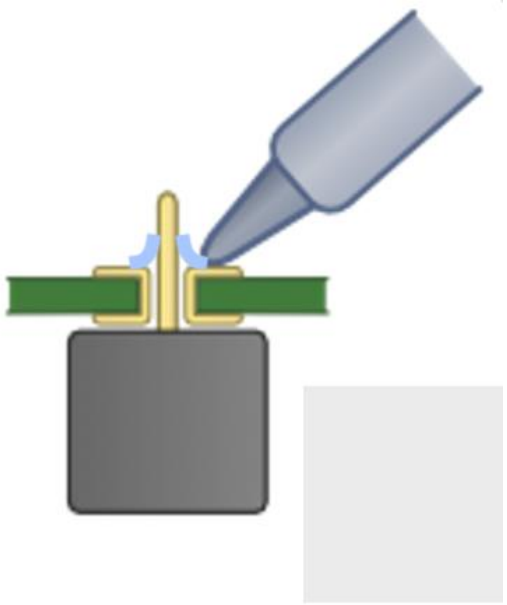
HYPERBITS™
cPCI Serial Space Connectors with S-FECT™ Technology



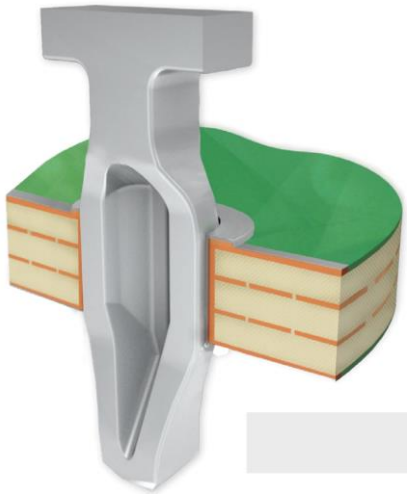
HYPERBITS CONNECTOR with S-FECT Technology



Why is HYPERBITS superior**?**



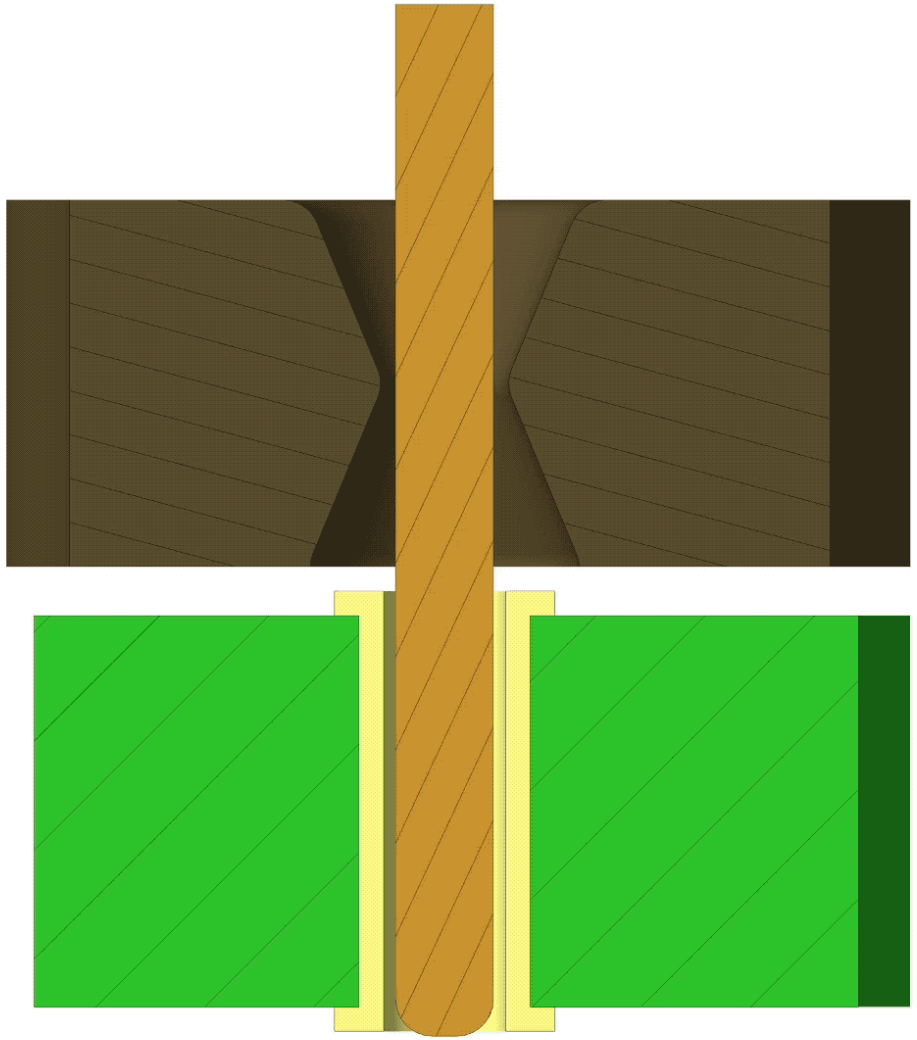
NO SOLDERING



NO PRESS-FIT

… **because it employs** S-FECT™ Technology

What is S-FECT Technology**?**



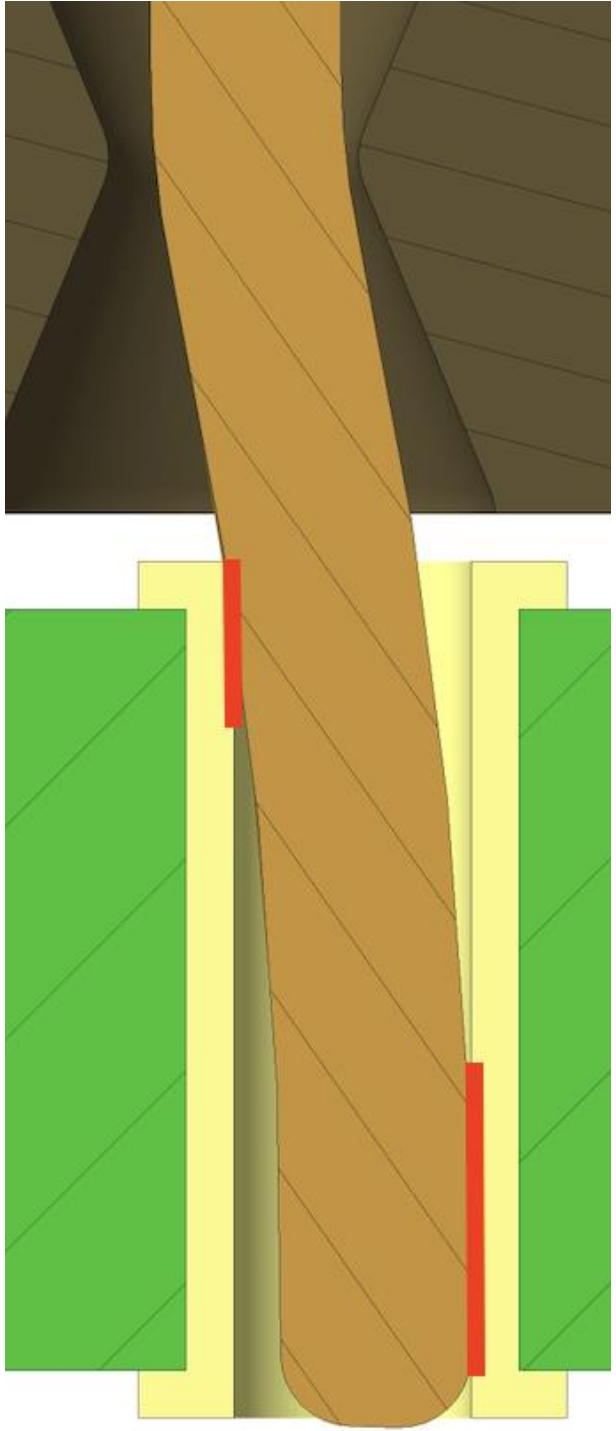
SLIDE-**F**IT
ELECTRICAL
CONTACT
TERMINATION

External Pressure Element

Technology

Already qualified to

Mil - 39029
GSFC-311
ESCC-3401



S-FECT

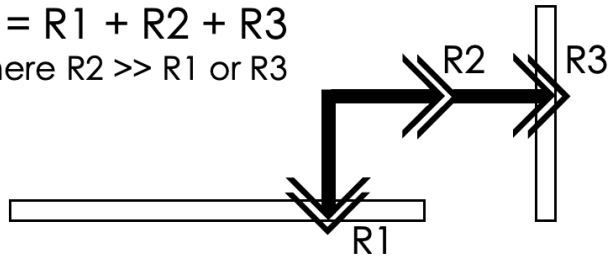
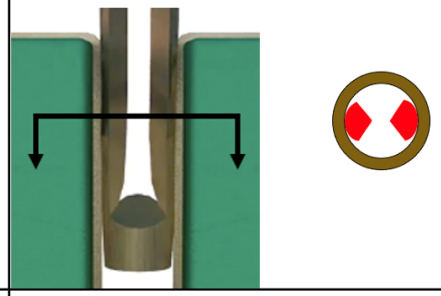
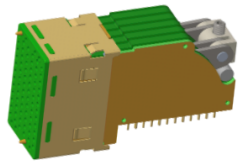
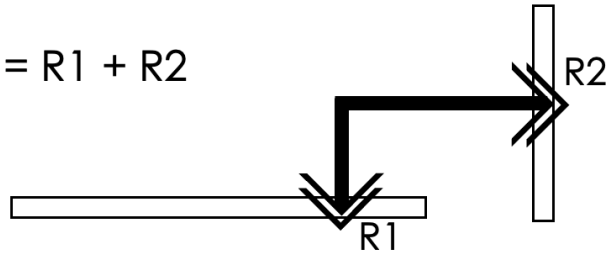
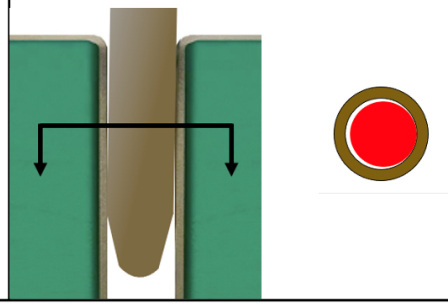
Technology

Similar mechanism of operation

<Higher normal Force

>Lower resistance

Advantages in S-FECT Technology?

Traditional Press-Fit Technology 	Cost of components and total installed cost:  Requires special assembly tooling	Total resistance PCB to PCB: **Rt** = R1 + R2 + R3 where R2 >> R1 or R3 	Increased current density in reduced cross-section: 
S-FECT™ Technology 	Cost of components and total installed cost:  No special assembly tooling required	Total resistance PCB to PCB: **Rt** = R1 + R2  Same logic applies to impedance	Constant current density in continuous cross-section: 

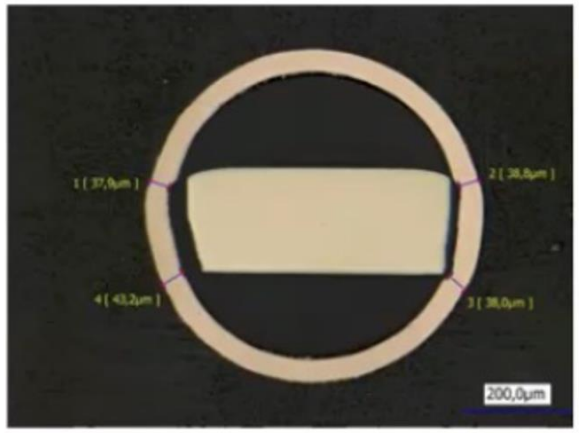
Single-piece connector which mates directly with the backplane!

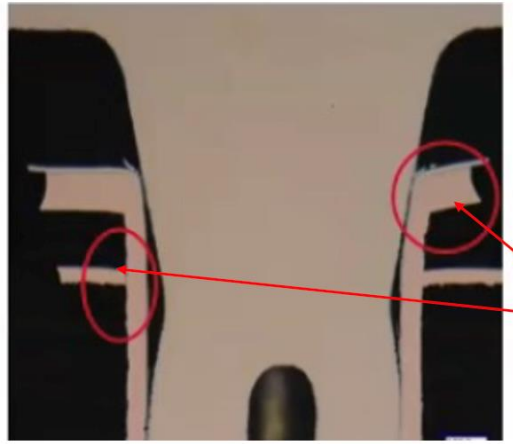
Advantages of S-FECT Technology compared to press-fit

- ZERO installation force
- ZERO specialty tools
- ZERO wiping on PTH
- ZERO jet effect
- ZERO deformation
- ZERO loose particles
- ZERO inspection

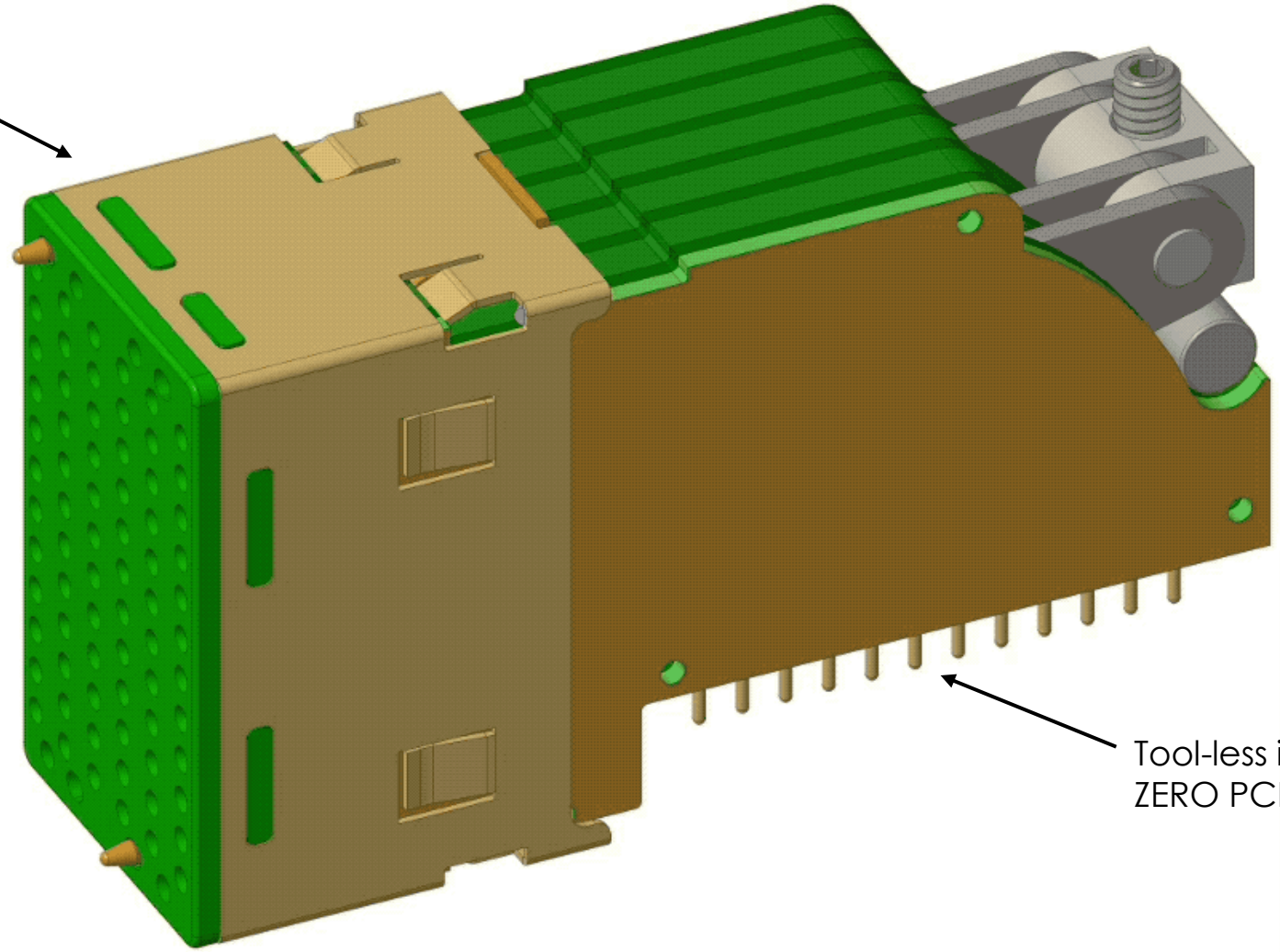
- MINIATURIZATION FRIENDLY
- SUPERIOR THERMAL BEHAVIOR
- LOWEST MANUFACTURING COST
- LOWEST INSTALLED COST

S-FECT technology eliminates unnecessary layer lift and deformation





HYPERBITS CONNECTOR with S-FECT Technology



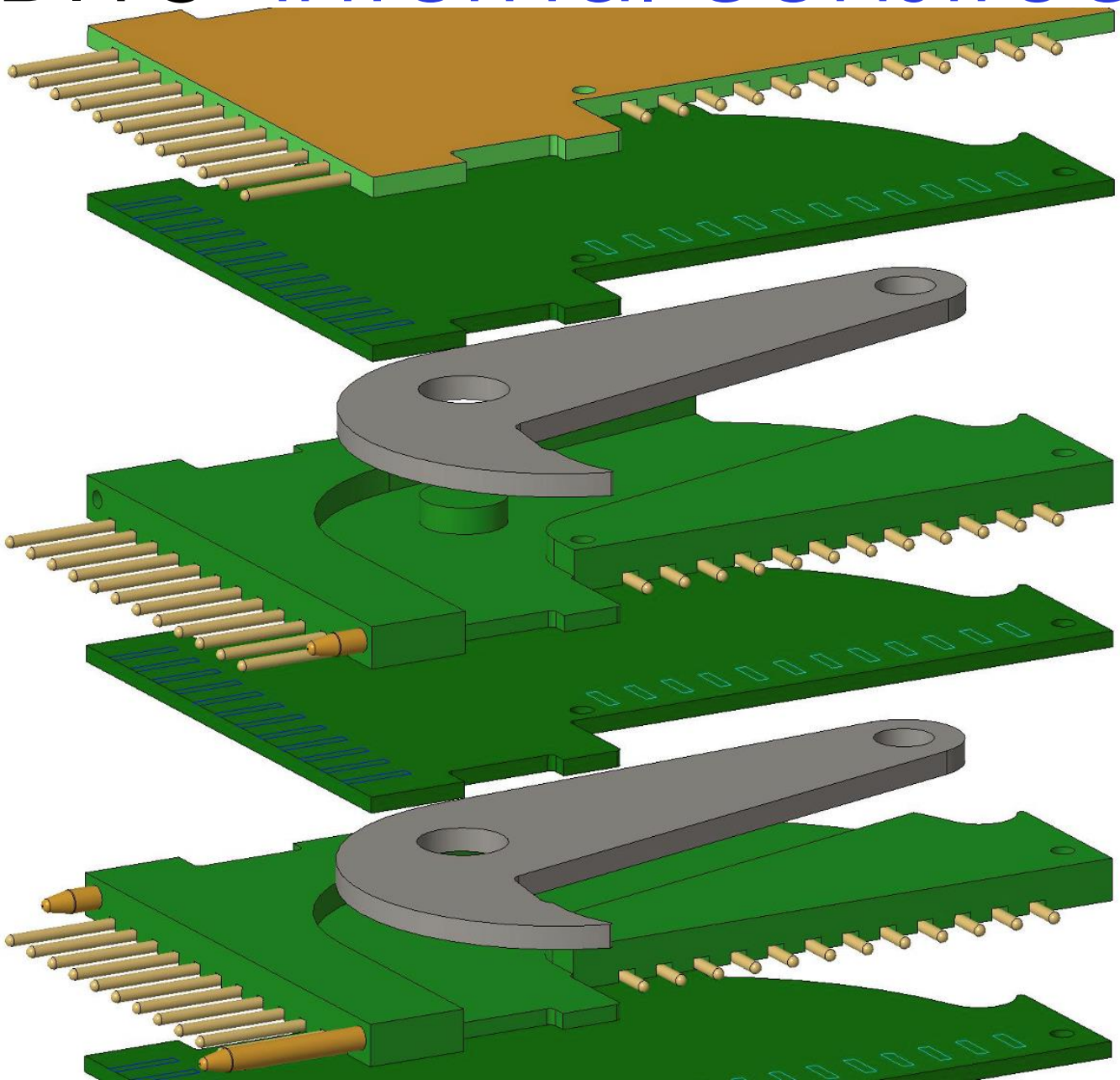
Blind-mating with protection faceplate and post-insertion offset system

Locking system

Tool-less installation and ZERO PCB insertion resistance

HYPERBITS internal construction

Connector body features composite construction with alternating layers of PCBs and spacers and an integrated mechanical locking system



HYPERBITS internal construction

state-of-the-art in materials performance

PROVEN PCB PERFORMANCE FOR SPACE APPLICATIONS

isola®

THE BASE FOR INNOVATION

Tachyon®100G
up to **110**Gbps

I-Tera® MT40
up to **50**Gbps

w w w. i s o l a – g r o u p. c o m

ISOLA PRODUCT SI PERFORMANCE RANGE

Product	Dk	Df	5 Gbps	10 Gbps	15 Gbps	20 Gbps	40 Gbps	60 Gbps	80 Gbps	100 Gbps
IS415	3.72	0.012								
IS415HR	3.80	0.012								
FR408	3.67	0.012								
FR408HR	3.68	0.092								
I-Speed	3.64	0.006								
TerraGreen	3.44	0.0039								
I-Tera MT40	3.45	0.0031								
Tachyon 100G	3.02	0.0021								

outgassing: TML 0.14%, CVCM <0.01%

- Full range of mid to ultra low loss products
- Robust resin technology for increased design density
- Complete range of constructions for design flexibility

Legacy
New

isola

HYPERBITS internal construction

state-of-the-art in materials performance

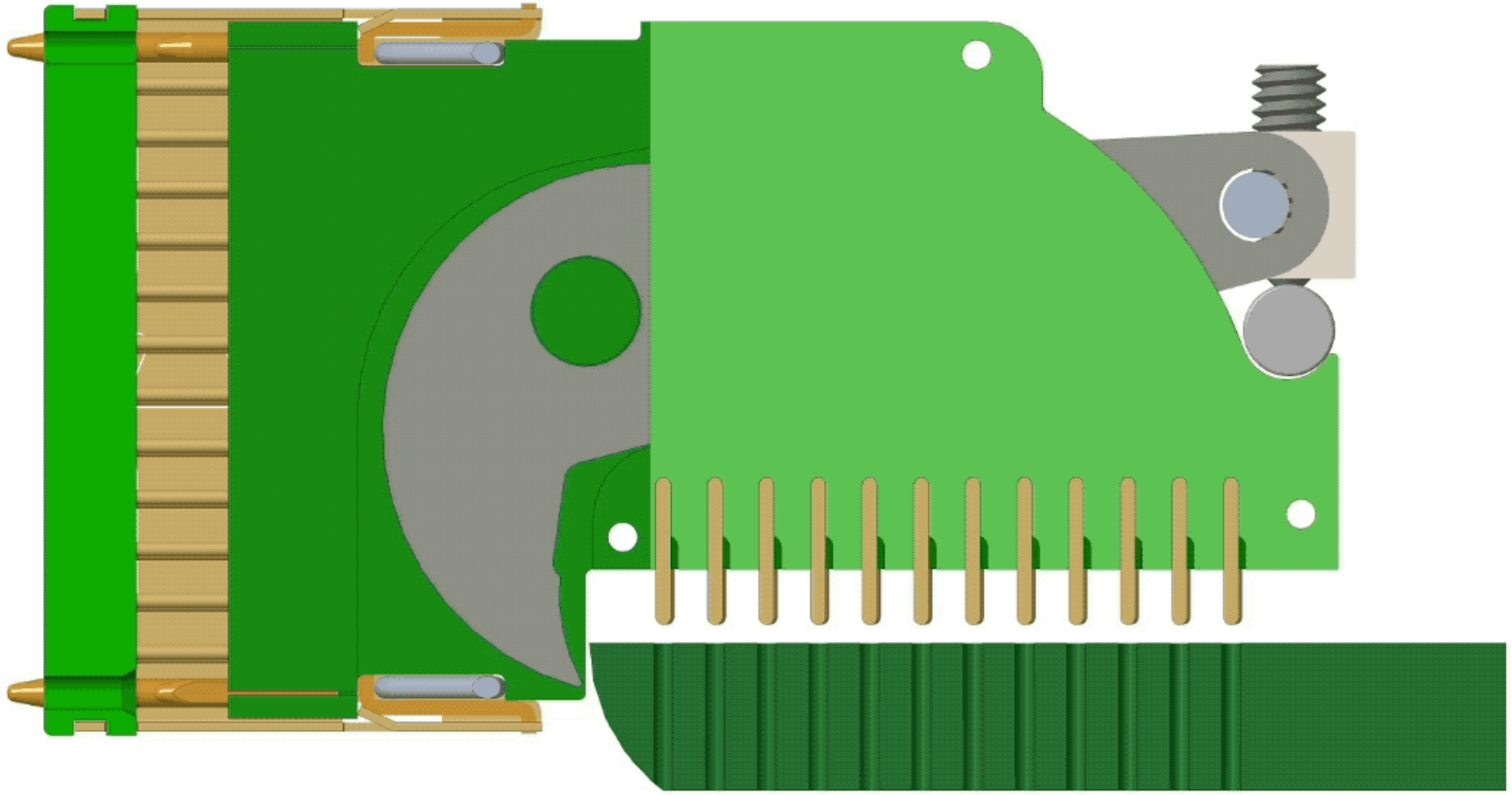
HIGH PERFORMANCE COPPER ALLOY

- **Superior flex-life**
- **Best in class conductivity**
- **Excellent mechanical strength**
- **Resistance to thermal softening**

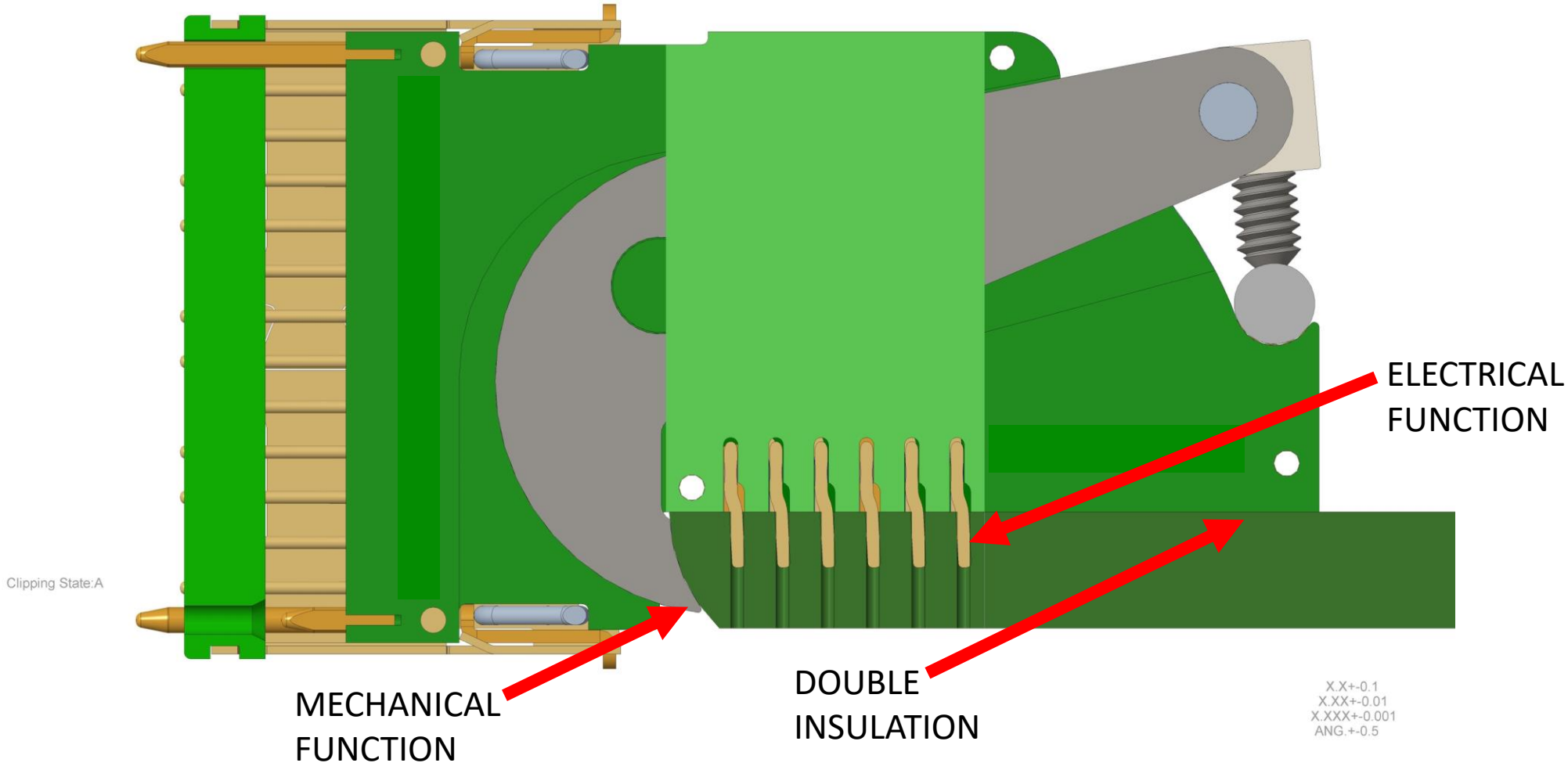
www.fiskalloy.com

HYPERBITS CONNECTOR card installation:

no tools, no soldering, only a hex driver…

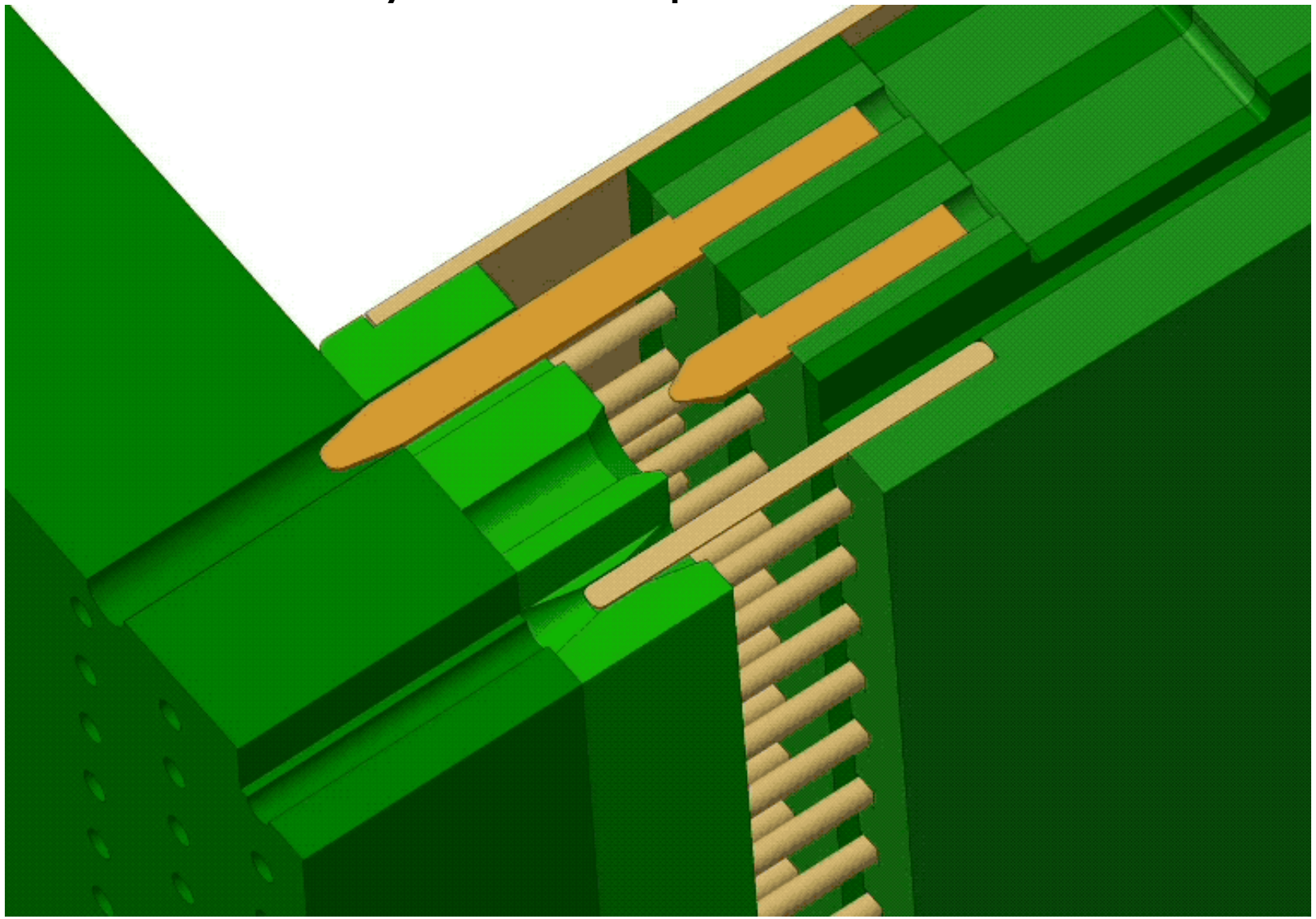


MECHANICAL FUNCTION fully separated from ELECTRICAL FUNCTION

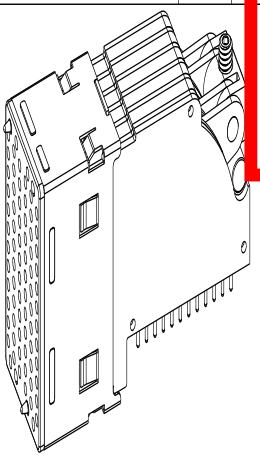


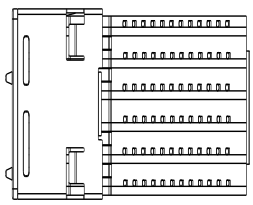
HYPERBITS CONNECTOR

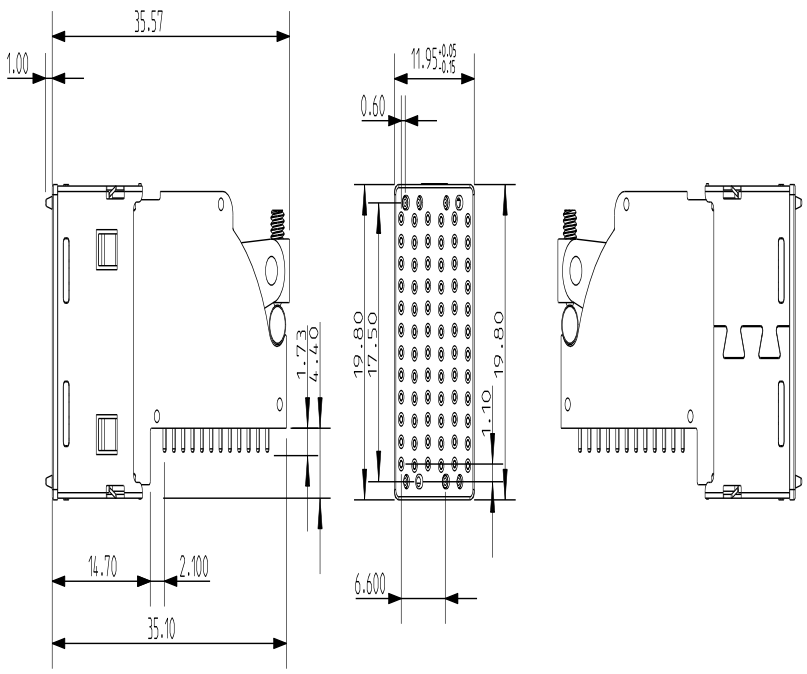
blind-mates directly with the backplane…

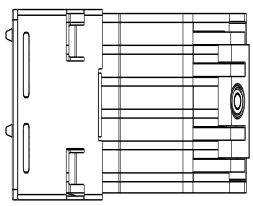


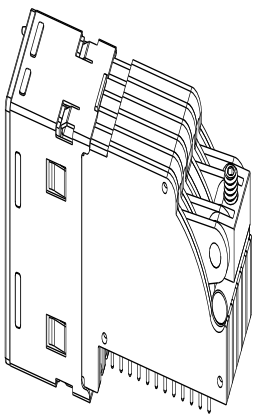
REV.	DESCRIPTION	DATE	APPROVAL
1	RELEASE FOR PROTO RUN	Mar-19-22	
2	RELEASE FOR PROTO RUN	MAY-23-22	
3	RELEASE FOR PROTO RUN	AUG-23-22	



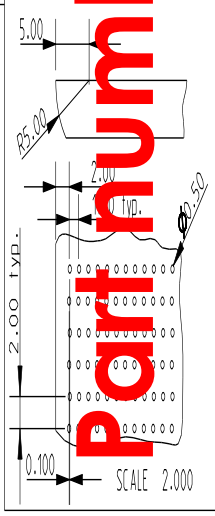








RECOMMANDED PCB LAYOUT



Part numbers released

UNLESS OTHERWISE SPEC.	APPROVAL	DATE	HYPERBITS™
DIMENSIONS ARE IN MM TOLERANCES ON WHOLE No. ± DECIMAL: .X ± .XX ± 0.10 .XXX ± 0.05 X/X ± ANGLE ± HOLE DIA.±0.08 MAXIMUM WARP 0.10 PER 100mm OF LENGTH	DRAWN	Mar-19-22	
	CHECKED		TITLE: HYPERBITS MECHANICAL OUTLINE
	PROJ.ENG.		
	MANUF.ENG.		
	Q.A.		
MATERIAL:	REMOVE ALL BURRS AND SHARP EDGES		SIZE: B PART NO. HYP1F600 REV. 3
FINISH: -	DO NOT SCALE DRAWING		SCALE: 40.000 SHEET 1 OF 1

REV.	DESCRIPTION	DATE	APPROVAL
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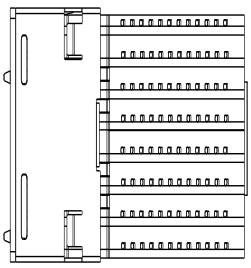
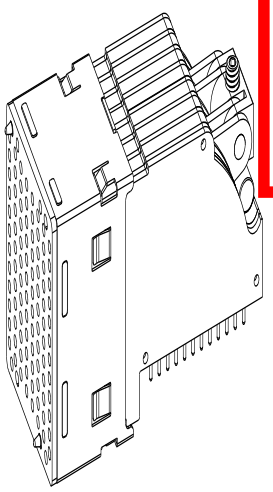
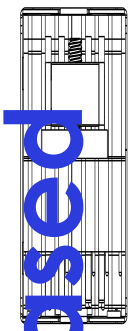
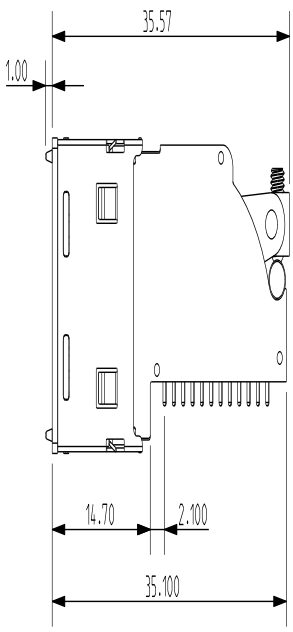
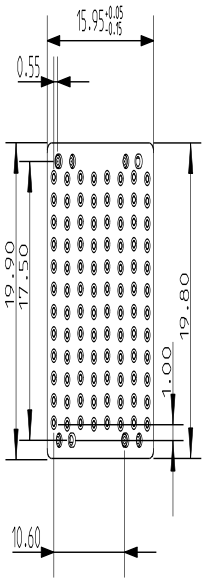
2	RELEASE FOR PROTO RUN	SUG-23-22	

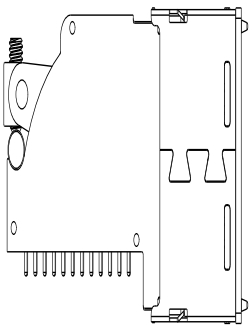


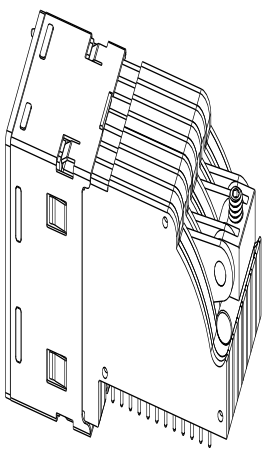


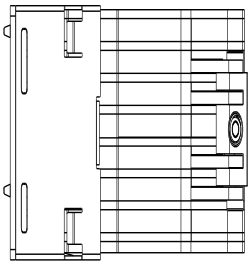










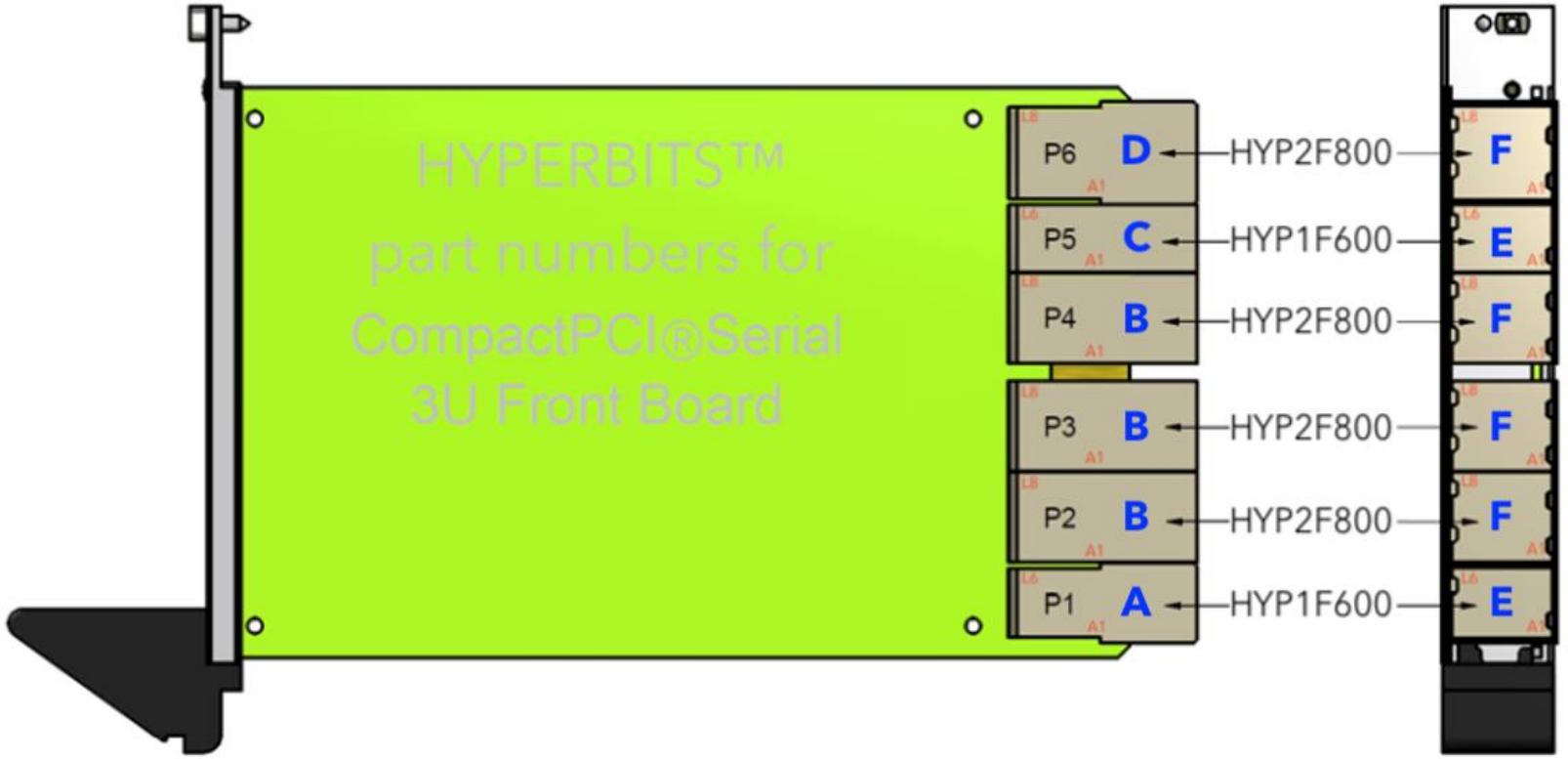


Part numbers released

UNLESS OTHERWISE SPEC.	APPROVAL	DATE	HYPERBITS™
DIMENSIONS ARE IN MM TOLERANCES ON WHOLE No. ± DECIMAL: .X ± .XX ± 0.10 .XXX ± 0.05 X/X ± ANGLE ± HOLE DIA.±0.08 MAXIMUM WARP 0.10 PER 100mm OF LENGTH	DRAWN	Mar-19-22	
	CHECKED		TITLE: HYPERBITS MECHANICAL OUTLINE 8 ROWS
	PROJ.ENG.		
	MANUF.ENG.		
	Q.A.		
MATERIAL:	REMOVE ALL BURRS AND SHARP EDGES		SIZE: B PART NO. HYP2F800 REV. 2
FINISH: -	DO NOT SCALE DRAWING		SCALE: 40.000 SHEET 1 OF 1

HYPERBITS™

2 part numbers replace 6 part numbers



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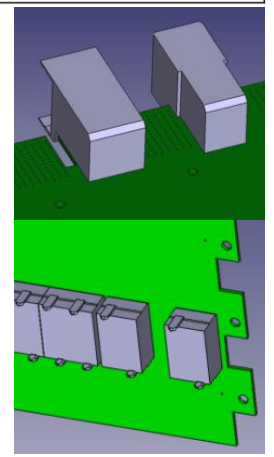
This section compares the

AIRBUS	ADS spec	Ref : DOC-EEE-000218505 Issue : 02 Rev. : 00 Date : 15/03/2021 Page : i

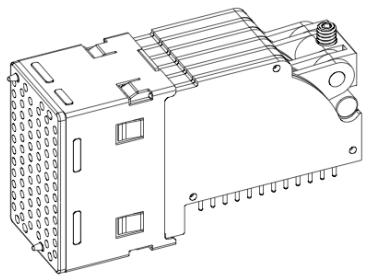
Front board connectors
with the following configurations:
6 columns x12 rows / 72contacts / 2 or 4 walls
8 columns x12 rows / 96 contacts / 2or 4 walls

Front backplane connectors
with the following configurations:
6 columns x12 rows / 72contacts
8 columns x12 rows / 96 contacts

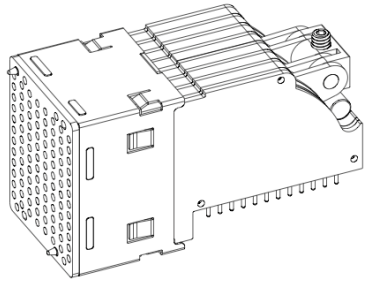


with the

HYPERBITS™ DESIGN SPECIFICATION



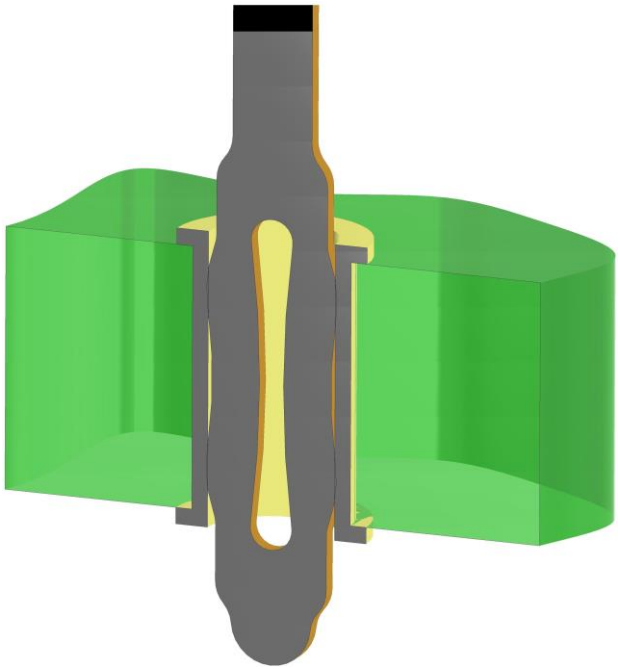
6 columns with
2mm pitch x 12 rows,
72 contacts,
24 differential pairs



8 columns with
2mm pitch x 12 rows,
96 contacts,
32 differential pairs

Description	ADS spec	HYPERBITS™ spec	Condition / Comments
Plating thickness on contacts:	**1.27µm** minimum	**1.27µm** minimum	electroplated gold per ESCC23500 §3.3
Materials of concern:	Pure tin (Sn)	Pure Tin (Sn) NOT PRESENT	Not allowed
Mass:	to be supplied by MANUF	TBD	**Value remains TBD**
Operating temperature range:	-55°C to +125°C	**-65**°C to +**155**°C	Qualification temperature range is -55°C to +125°C
Marking	part number, date code	part number, date code	engraved or laser marked
Mating/Unmating cycles a)backplane b)card	500 cycles	1000 operations with a&b	Value tbd with MANUF per ESA/ESCC 3401 § 9.18
Mating/Unmating Force/contact a)backplane b)card	M 0.45N.st to 0.60N / U ≥0.15N	a) 0.6N max b) 0.01N	Per ESA/ESCC 3401 § 9.20 Mated and unmated 4 times **S-FECT ADVANTAGE**
Contact retention 5 pcs or 20% to be tested	4.4N for 6 sec.	4.4N for 6 sec.	ESA/ESCC 3401 § 9.17
Axial displacement MAX 0.3mm	10N for 6 sec.	10N for 6 sec.	ESA/ESCC 3401 § 9.17
High Speed Data Rate:	25 Gbps	**25 Gbps – phase 1**	Differential signaling **phase 2: 35 Gbps phase 3: 56 Gbps phase 4: 100 Gbps**
Differential impedance:	**100Ω**	**Max 105Ω – Min 95Ω**	**+/- 5% target: 95Ω min and 105Ω max**
Contact resistance between mated contacts	20 mΩ	Not Applicable	ESA/ESCC 3401 § 9.1.1.3
Contact resistance between press-fit pin to PCB	300 µΩ MAX	Not Applicable	IPC 9797 §4.3.4 Test Method IEC 60512 test Method 2a. Measured during Qualification
Contact resistance between Slide-Fit Pin and PCB		≤ 4mΩ	**with a)backplane and with b)card**
Maximum resistance per line measured PCB to PCB	≤ 20.6mΩ	**≤ 10mΩ 50% improvement**	**From trace on backplane to trace on card including interfaces**
Current rating per contact:	**2A**	**2A**	1A minimum derated current over temperature range. **2A all contacts under load with maximum 35°C temperature rise, 1.6A continuous all contacts @30°C rise**
Working voltage	28V	**96V at any altitude**	
Insulation resistance	1 GΩ min	1 GΩ min	ESA/ESCC 3401 § 9.1.1.1 Test Method IEC 512-2, Test 3a, Method B. 500V +/- 50V
DWV	750 VRMS	750 VRMS	**Between PCBs**
Corona Effect	15VRMS	15VRMS	at 33000m per IEC-68-2-13
Back-drilling compatibility a)backplane b)card	required	**a) YES b) YES**	**MIN 1.6mm via depth from top of PCB**
S-Parameters – Insertion Loss – Cross talk – Capacitance – Inductance – Propagation Delay: **Targets provided in specification Actual values for HYPERBITS are TBD**			

Note: 3 REWORKS & Repairability requirement



Hard-compliant press-fit is damaging to PTH

9 PRESSFIT SPECIFICATION

It shall be noted that ECSS-Q-70-61 is being amended to cover the assembly verification for solderless solutions except press-fit but can still apply: mate/demate , 3 reworks, vibration (+electrical monitoring), shock (+electrical monitoring), damp heat (+electrical monitoring), 500 thermal cycles + microsections and 2000h Life test.

Test item		Parameter	Test Method	ESA/ESCC Requirements
Spring force measurements		The manufacturer shall procure a certificate of compliance to this	As per IPC 9797 §4.2.4	IPC specific, Not defined by ESCC3401
Compliant Pin Insertion Force		Acceptable criteria : meet the manufacturer requirement	As per IPC 9797 § 4.3.1	IPC specific, Not defined by ESCC3401
Compliant Pin Retention Force		Acceptable criteria : meet the manufacturer requirement	As per IPC 9797 § 4.3.5	IPC specific, Not defined by ESCC3401
PCB Hole deformation radius		Cross-section: • Below 70µm of deformation • At lest 8µm of copper remaining	As per IPC 9797 §4.3.6	IPC specific, Not defined by ESCC3401
PCB Hole wall Damage		Cross-section • Deformation lower than 100µm • No cracks or whites marks (darkfield)	As per IPC 9797 §4.3.6	IPC specific, Not defined by ESCC3401
Reparability		Mandatory: the connector should be replaced at least one time The target is 3 times. Procedure and tooling to be described by the manufacturer.	To be discussed with the manufacturer	Not defined by ESCC3401
Plating Thickness **(Plated-Through Hole Copper Thickness)**		.2.1.4 Plated-Through Hole Copper Thickness Absolute minimum 25 pm [984 pin[• Absolute maximum 55 pm [2165 pin] • Minimum average 33 im [1299 pin] • Diameter e of finished) hole X, 0 of drilled hole Y: — X = Y — 0,085 mm [0.003 in] — tor 0.5 mm [0.02 in] X 0.8 mm [0.031 in]: tolerance of X ± 0.04 mm [0.0015 in] — for 0.8 mm [0.031 in] <X 2.2 mm [0.087 ml: tolerance of X ± 0.05 mm [0.002 in] 3.2.3 Surface Finish Common surface finishes tor press-flt applications arc: • Immersion Sn: 1.0 - 1.5 pm [39 - 59 pin) •.Immersion Ag: 0.1 - 0.5 .µm [3.9 - 20 pin] • OSP: 0.2 - 0.5 ijm [7.9 - 20 pin] • ENlG: — Ni: 3 - 7 pm [118 - 276 pin], and — Immersion Au: 0.05 - 0.1 pm [1.2 - 3.9 µin]	As per IPC 9797 §3.2.1.4 for copper And § 3.2.3 for surface finish if different thicknesses are qualified AABUS shall be agreed.	IPC specific, Not defined by ESCC3401
Pressfit hole annular ring Annular		3.2.1.3 Minimum Annual Ring Minimum annular ring after etching should be at least 0.15 mm [0.006 in].	As per IPC 9797 § 3.2.1.3	IPC specific, Not defined by ESCC3401
Backdrilling compatibility		Yes/No ?	If yes please specify the min nominal remaining hole length with min/max tolerances.	

1 Background

2 Solution

3 Specification

4 Test Plan

5 Conclusion

ALTER
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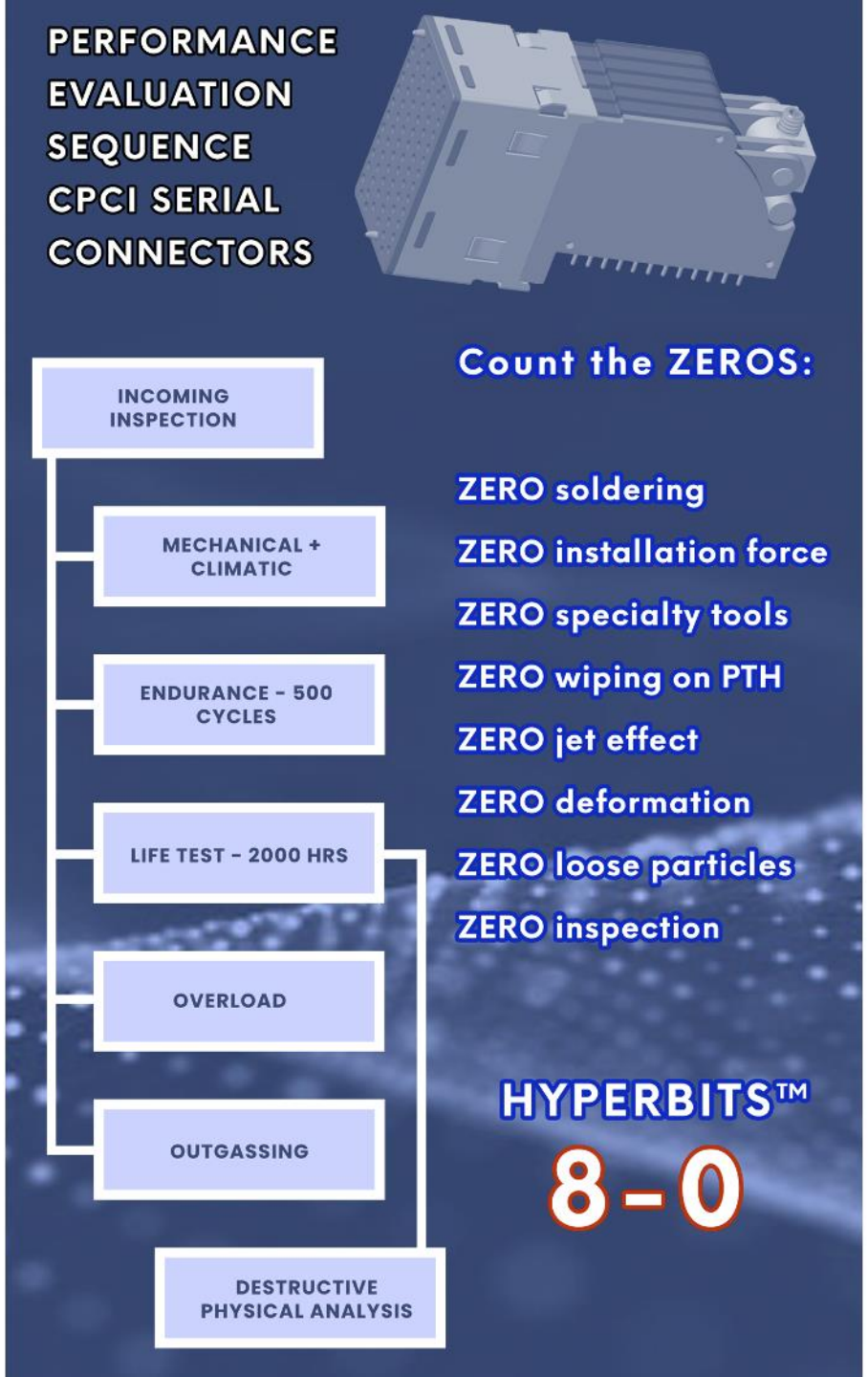
HYPERBITS™ Connector Design and Qualification For High Reliability Compact PCI Serial Space Applications

(Part II: Evaluation Activities)

Prepared by **Dimas J. Morilla Mairén**,
Technical Support Manager

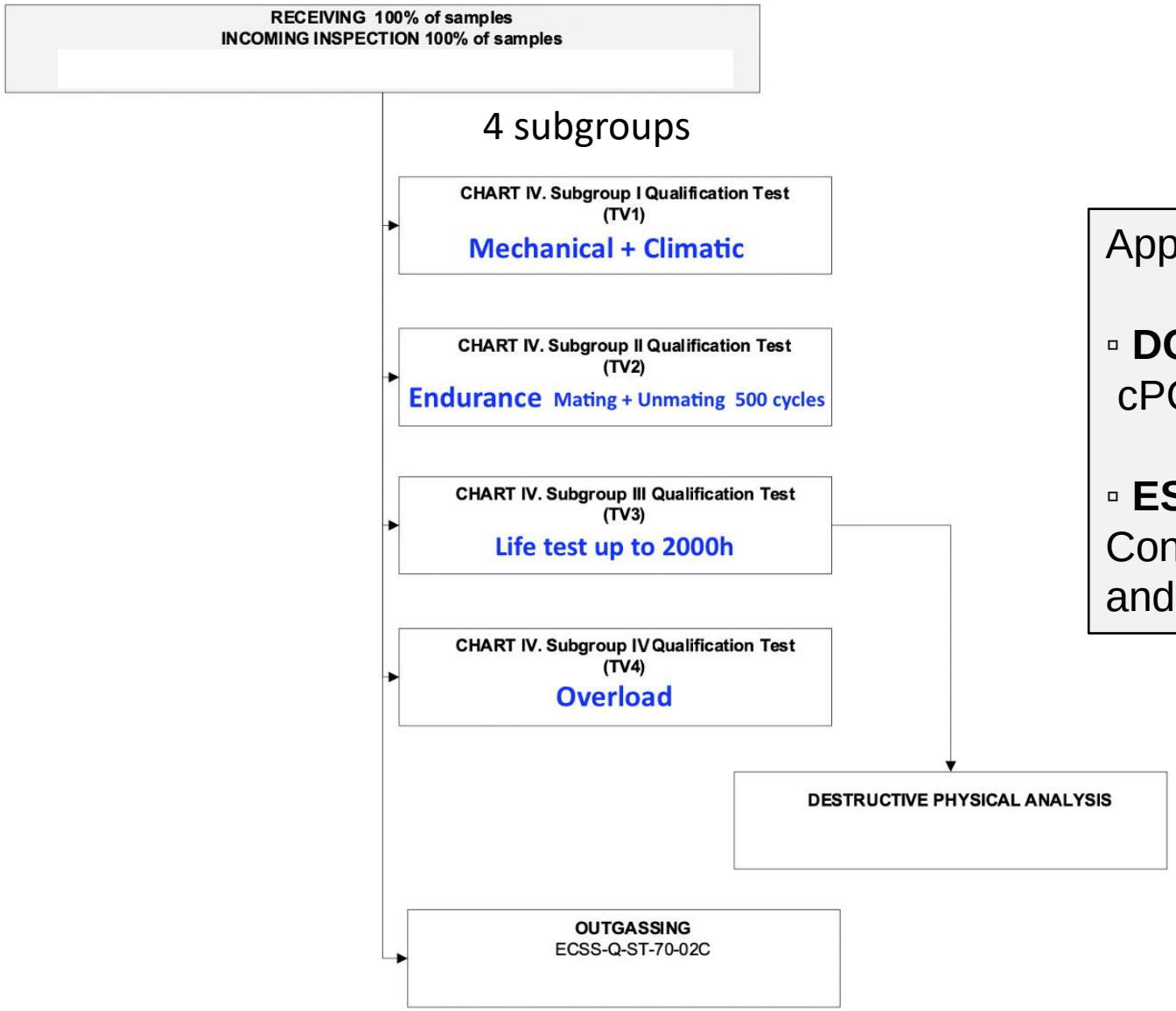


INTRODUCTION

The **evaluation activities shall start in December of 2022**.
Note: the following **information may be updated** before that date.

This exercise will represent a significant first step in the path towards the full qualification of interconnect devices for CPCI Serial Space systems.

TEST FLOW

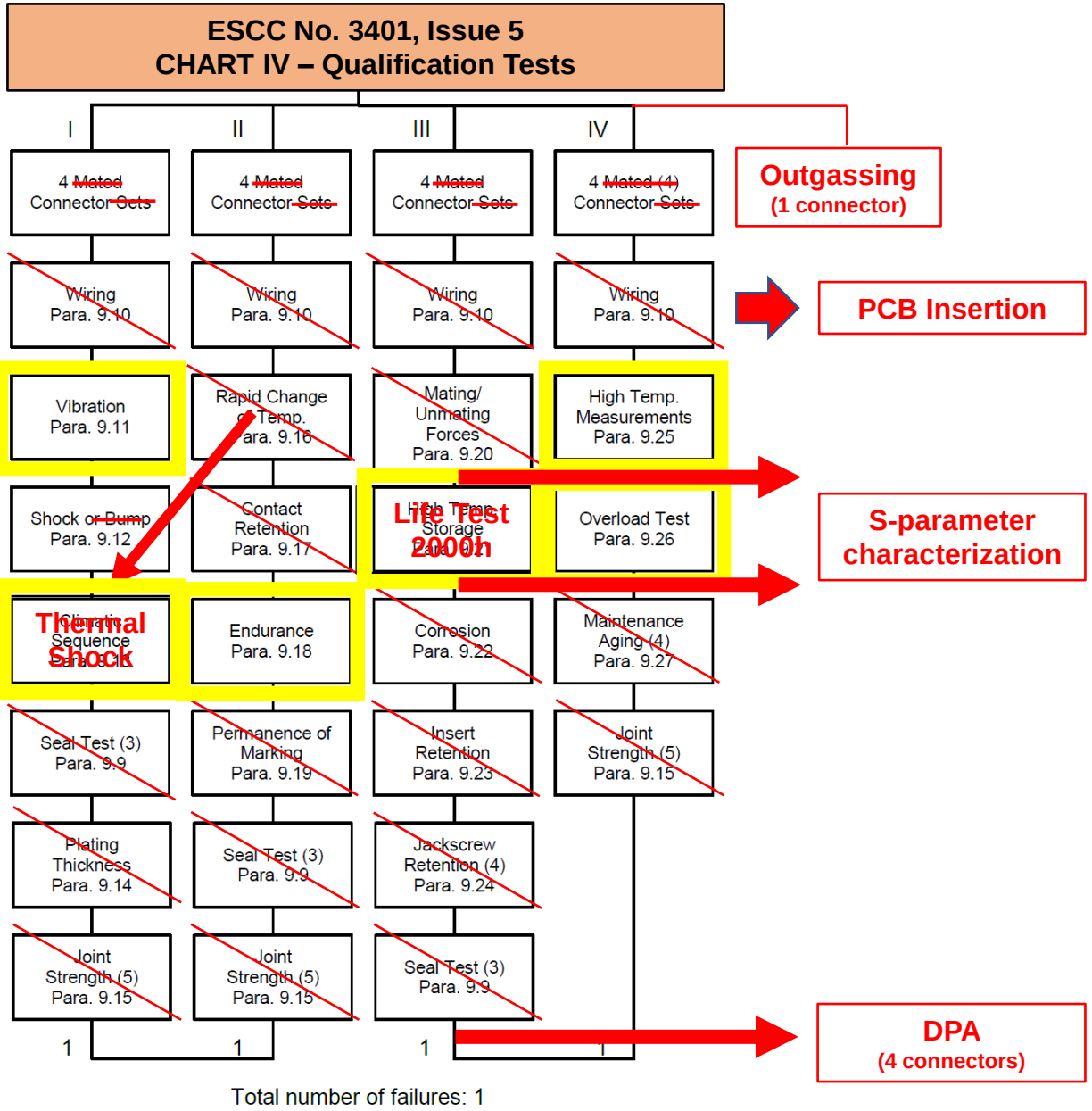


Applicable documents:

- **DOC-EEE-000218505, Issue 2**
  cPCI Serial Connector for Space

- **ESCC Generic Specification No. 3401**
  Connectors, Electrical Non-Filtered, Circular and Rectangular

CHART IV – QUALIFICATION TESTS: DEVIATIONS



1.- ALTER Technology suggested to include an **Outgassing** test as this may be one of the most critical points.

2.- Microsection is not performed after Subgroup I. In the specification document with ref. DOC-EEE-000218505, Issue 2, this is requested as part of the Assembly Verification. Anyway, ALTER Technology has included a **Destructive Physical Analysis** (covering Cross Section) to be performed on samples subjected to the previous CHART IV – Qualification Tests – Subgroup III (Life Test).

3.- A biased Life Test is missing. **2000h Life Test** is requested as part of the Assembly Verification in the specification document with ref. DOC-EEE-000218505, Issue 2. Environmental specification and ESCC 3401 only consider High Temperature Storage test.

ALTER Technology proposed to replace the High Temperature Storage test of Subgroup III by a biased Life Test at 125ºC. Intermediate measurements (S-parameters) at room, high and low temperatures were included after 500h and 1000h.

4.- Rapid Change of Temperature (**Thermal Shock**) was reallocated from Subgroup II into Subgroup I, replacing Climatic Sequence Dry Heat and Damp heat Accelerated tests.

CHART IV – QUALIFICATION TESTS SUBGROUP I (TV1)

ALTER TECHNOLOGY

N.º	TEST	SAMPLES	TEST METHOD
1	External Visual Inspection	4 + control	ESCC 20500
2	PCB Insertion	4 + control	TBD (Note 1)
3	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
4	External Visual Inspection	4 + control	ESCC 20500
5	Sine Vibration	4	ESCC 3401 Par. 9.11 (Notes 2 & 3)
6	External Visual Inspection	4 + control	ESCC 20500
7	Random Vibration	4	ESCC 3401 Par. 9.11 (Notes 2 & 4)
8	External Visual Inspection	4 + control	ESCC 20500
9	Mechanical Shock	4	ESCC 3401 Par. 9.12.1 (Notes 2 & 5)
10	External Visual Inspection	4 + control	ESCC 20500
11	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
13	Thermal Shock	4	TABLE III of Test Plan
14	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
15	External Visual Inspection	4 + control	ESCC 20500

1.- IPC Class 3 requirements shall be preferred for PCB manufacturing.

Details on mounting shall be provided by manufacturer in each case. In the absence of those, insertion speed shall be between 25 mm/min and 50 mm/min as per NF EN60352-5, Para. 5.2.2.2.

2.- No impedance change or discontinuity of 1 ns or longer duration in accordance with EIA-364-87.

3.- Sinusoidal Vibration
- Frequency range: 10-2000-10 Hz.
- Entire range from 10 Hz to 2000 Hz and return to 10 Hz in 30 mn.
- Amplitude: 1,5mm or 20g whichever is less.
- The cycle shall be performed in 3 mutual perpendicular direction total period of approximately 90 minutes.

4.- Random Vibration
- Fda f1= 20 Hz
- f2 = 2000 Hz
- ASD of 0,2 g2/Hz
- Total test period 30 minutes
- The cycle shall be performed in 3 mutual perpendicular direction total period of approximately 90 minutes.

5.- Mechanical Shock
- Shape of shock pulse: half-sine.
- A peak acceleration of 50 g with an 11 ms duration pulse.
- 3 shocks in each direction along the 3 mutually perpendicular directions (i.e. 18 in total).

CHART IV – QUALIFICATION TESTS SUBGROUP I (TV1)

ALTER TECHNOLOGY

Table II of ATN-SC-1013: Electrical Measurements at Room Temperature

N.º	TEST		CONDITIONS (T_A = 25 ºC)	LIMITS		UNIT
				MIN.	MAX.	
1	R_C	Contact Resistance	TBC	TBC	TBC	mOhm
2	V_P	Voltage Proof	TBC	TBC	TBC	--
3	R_I	Insulation Resistance	TBC	TBC	TBC	MOhm

1.- Parameters, conditions and limits are TBC depending on the test vehicle definition.

Table III of ATN-SC-1013: Conditions for Thermal Shock

NUMBER OF CYCLES: 20		
STEP	TEMPERATURE	TIME
1	-55 ºC (+0, -10)	≥10 min
2	125 ºC (+15, -0)	≥10 min

CHART IV – QUALIFICATION TESTS SUBGROUP II (TV2)

ALTER TECHNOLOGY

N.º	TEST	SAMPLES	TEST METHOD
1	External Visual Inspection	4 + control	ESCC 20500
2	PCB Insertion	4 + control	TBD (Note 1)
3	External Visual Inspection	4 + control	ESCC 20500
4	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
5	Endurance until 50 times (Note 3)	4	ESCC 3401 Par. 9.18 (Note 2)
6	Electrical Measurement at Room Temperature	4 + control	TABLE II of test Plan
7	Endurance until 500 times	4	ESCC 3401 Par. 9.18 (Note 2)
8	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
9	External Visual Inspection	4 + control	ESCC 20500

1.- IPC Class 3 requirements shall be preferred for PCB manufacturing.

Details on mounting shall be provided by manufacturer in each case. In the absence of those, insertion speed shall be between 25 mm/min and 50 mm/min as per NF EN60352-5, Para. 5.2.2.2.

2.- Test conditions: 500 Cycles. A cycle is defined as one mating and one un-mating. The coupling means shall be operated in a manner to simulate actual service. The plug and receptacle shall be completely separated during each cycle. The mating/unmating speed shall be 5 mm/second maximum and the cycling rate shall be 8 cycles/minute maximum.

3.- Number of cycles for intermediate measurement of endurance test is TBC.

CHART IV – QUALIFICATION TESTS SUBGROUP III (TV3)

ALTER TECHNOLOGY

N.º	TEST	SAMPLES	TEST METHOD
1	External Visual Inspection	4 + control	ESCC 20500
2	PCB Insertion	4 + control	TBD (Note 1)
3	External Visual Inspection	4 + control	ESCC 20500
4	Electrical Measurements at Room Temperature	4 + control	TABLE VII of Test Plan
5	Electrical Measurements at High Temperature	4	TABLE VIII of Test Plan
6	Electrical Measurements at Low Temperature	4	TABLE IX of Test Plan
7	Life Test (until 500 h)	4	TABLE VII of Test Plan
8	Electrical Measurements at Room Temperature	4 + control	TABLE VII of Test Plan
9	Electrical Measurements at High Temperature	4	TABLE VIII of Test Plan
10	Electrical Measurements at Low Temperature	4	TABLE IX of Test Plan
11	Life Test (until 1000 h)	4	TABLE VII of Test Plan
12	Electrical Measurements at Room Temperature	4 + control	TABLE VII of Test Plan
13	Electrical Measurements at High Temperature	4	TABLE VIII of Test Plan
14	Electrical Measurements at Low Temperature	4	TABLE IX of Test Plan
15	Life Test (until 2000 h)	4	TABLE VII of Test Plan
16	Electrical Measurement at Room Temperature	4 + control	TABLE VII of Test Plan
17	Electrical Measurements at High Temperature	4	TABLE VIII of Test Plan
18	Electrical Measurements at Low Temperature	4	TABLE IX of Test Plan
19	External Visual Inspection	4 + control	ESCC 20500

N.º	TEST	SAMPLES	TEST METHOD
1	External Visual Inspection	4	ESCC 20500
2	Lead Material Verification (Note 1)	1	ESCC 20500
3	Radiographic Inspection	4	ESCC 20900
4	Marking Permanence	4	ESCC 24800
5	Cross Section (Note 2)	4	ESCC 20400

Destructive Physical Analysis

1.- IPC Class 3 requirements shall be preferred for PCB manufacturing.

Details on mounting shall be provided by manufacturer in each case. In the absence of those, insertion speed shall be between 25 mm/min and 50 mm/min as per NF EN60352-5, Para. 5.2.2.2.

CHART IV – QUALIFICATION TESTS SUBGROUP III (TV3)

ALTER TECHNOLOGY

Table VI of ATN-SC-1013: Conditions For Life Test

N.º	CHARACTERISTIC	SYMBOL	CONDITION	UNIT
1	Duration	t	2000	h
2	Ambient temperature	T_A	125	ºC
3	Rated Current	I_{rated}	2	A

Tables VII, VIII and IX of ATN-SC-1013: Electrical Characterization at Room (+25ºC), High (+125ºC) and Low (-55ºC) Temperatures

N.º	TEST		CONDITIONS	LIMITS		UNIT
				MIN.	MAX.	
1	Z_{diff}	Differential impedance	Between two adjacent pins.	95	105	Ohm
2	IL	Insertion loss	Up to 3.12GHz	--	1	dB
			Up to 6.25GHz	--	1.5	dB
			Up to 12.5GHz	--	2	dB
3	$Xtalk_{near}$	Cross talk (Near end pins)	Up to 3.12GHz	--	-39	dB
			Up to 6.25GHz	--	-34	dB
			Up to 12.5GHz	--	-29	dB
4	$Xtalk_{far}$	Cross talk (Far end pins)	Up to 3.12GHz	--	-42	dB
			Up to 6.25GHz	--	-34	dB
			Up to 12.5GHz	--	-26	dB

1.- Parameters, conditions, and limits are TBC depending on the test vehicle definition. Values are given as target.

S-parameters were proposed to be performed in an independent subgroup because the design requirements for this measurement are completely different to those required for environmental testing. Differential pair routing is compulsory to properly characterize S-parameters, while for environmental test, contact shall be connected in series for electrical monitoring. This fact, together with the high number of contact count, makes the design of both PCBs completely different and no compatible one with another.

For this reason, the S-parameters characterization will be performed as part of Subgroup III (TV3) replacing the current electrical characterization.

CHART IV – QUALIFICATION TESTS SUBGROUP IV (TV4)

ALTER TECHNOLOGY

N.º	TEST	SAMPLES	TEST METHOD
1	External Visual Inspection	4 + control	ESCC 20500
2	PCB Insertion	4 + control	TBD (Note 1)
3	External Visual Inspection	4 + control	ESCC 20500
4	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
5	High Temperature Measurements	4	TABLE XII of Test Plan
6	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
7	External Visual Inspection	4 + control	ESCC 20500
8	Overload Test	4	TABLE XI of Test Plan
9	Electrical Measurement at Room Temperature	4 + control	TABLE II of Test Plan
10	External Visual Inspection	4 + control	ESCC 20500

1.- IPC Class 3 requirements shall be preferred for PCB manufacturing.

Details on mounting shall be provided by manufacturer in each case. In the absence of those, insertion speed shall be between 25 mm/min and 50 mm/min as per NF EN60352-5, Para. 5.2.2.2.

CHART IV – QUALIFICATION TESTS SUBGROUP IV (TV4)

ALTER TECHNOLOGY

Table XI of ATN-SC-1013: Conditions For Overload Test

N.º	CHARACTERISTIC	SYMBOL	CONDITION	UNIT
1	Duration	t	10	min
2	Ambient temperature	T_A	25	ºC
3	Rated Current	$I_{CURRENT}$	Note 1	A

1.- A current of 1.5 times the rated current specified in the manufactures for each contact size shall be passed through all contacts for a period of 30 seconds. This shall be followed by a period of 90 seconds with no current flowing. This shall constitute 1 cycle. The cycle shall be repeated 5 times (10 minutes total).

Table XII of ATN-SC-1013: High Temperature Measurements

N.º	CHARACTERISTIC	SYMBOL	CONDITION	UNIT
1	Duration	t	30	Min.
2	Ambient temperature	T_A	+125	ºC
3	Bias Voltage	V_{BIAS}	Not Biased	--

THANK YOU FOR YOUR ATTENTION

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ALTER TECHNOLOGY

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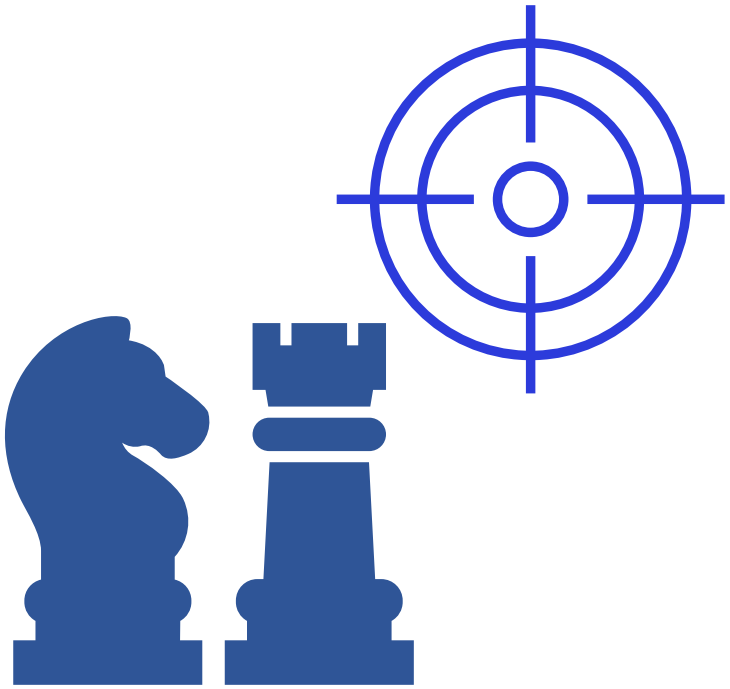

The Future of S-FECT Technology:

1: MINIATURIZATION – contact diameters feasible to 0.02mm ultra-fine diameter

2: IMPROVED POWER Transfer – for high power microprocessors & transfer through small footprint

3: Thermal Transfer through connector – important need to manage thermal build-up

S-FECT™ Technology will contribute to the **advancement** of harsh environment electronics architectures with significant advantages:

SIMPLE IMPLEMENTATION | **LOW COST** | **HIGH RELIABILITY**

HYPERBITS™

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NOW AVAILABLE FOR LICENSING AGREEMENT

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Questions?

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MINDREACH

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