PACKAGING FOR HIGHLY DISSIPATING DIES ON PCBS

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INTRODUCTION

Semiconductor used on the new generations of digital equipment presents fine device features (e.g. 65 nm), high I/O count (Up to 2000's I/O) and fast clock rates (3-10GHz). These new technologies must handle higher data rates resulting in higher dissipated power and in tighter requirements on parasitic effects caused by current packages. For today's solutions, the packages are based on a solution where the die is assembled upside-down (flip chip technology) and with the heat sink glued on top. The ceramic package with large dimensions as 45mm x 45mm induces high mismatch of CTE between package and PCB. Thus the reliability of the assembly is managed by using soldered columns able to support the thermomechanical stresses. The solderless interposer assembly can be envisaged as alternative solution subject to guarantying a high reliability under harsh environment (vibration, thermal-cycling), and whilsr achieving electrical performance at high data rate (6.25 Gbps) thanks to high quality of contact.
In this context, Thales Alenia Space and Smith Interconnects have started the activity to develop and assess a solderless interconnect system for high pin count package on PCB for high speed applications. In the frame of this activity, the following sequential tasks were conducted:

- State-of the art review on solderless interconnection solution and cooling system
- Definition of requirements and Trade-off
- Definition and design of the interposer system
- Assembly of the test vehicles and test campaigns
- Test results
- Limitations & recommendations

STATE-OF THE ART REVIEW

Initially, a review of the state of the art on high speed, high dissipated power, high pin count solderless solutions was done. Five interposer families were identified. For each of them, the different technologies on the market were presented:

- Conductive Elastomer based (Silmat™, Metal contact interposer from Shin-Etsu Polymer, Anisotropic conductive sheet from Shin-Etsu Polymer…) ,
- Bending beam based (InterCon cLGA® from Amphenol, iQ® from Cinch…),
- Rocking beam based (ROL™100A from Johnstech, Kalypso from Antares advanced test technologies, ZIGMA™ from JF technology Berhad…),

- Spring based (RC Connect-R™ from Ardent Concepts, RC Scrub-R™ from Ardent Concepts, Hymstac interposer from Smiths Interconnect-Hypertac; Spring Contact RF Probe from Smiths Interconnect-Hypertac/Smiths Connectors…) ,
- Random wire bundle based (CIN::APSE® from Cinch)

Then, a review of the cooling system was carried out. The increase of the I/O induces an increase of the power density at component level (at least 15 Watt) and at higher level (board/equipment/satellite panel). Because of these constraints, the existing thermal control technics based on common sequential PCB are not able to provide competitive architectures. New thermal management solutions were proposed and considered:

- Through Board Thermal Control : Thermal control through the assembly of the component and the board:
  - Partially suppression of the board underneath the component (PCB windows)
  - Thermal vias (macro or micro vias)
  - New PCB material : an higher thermal dissipative raw material
- Direct Thermal Control : Thermal control from the top the component
  - Miniature Heat Pipe System (MHP);
  - Mini Loop Heat Pipe;
  - Aluminum encapsulated (APG)

From flip-chip based components, DTC is very advantageous. Indeed, the power can be directly dissipated via the back of the die near the active area. Considering the background of TAS and the potential performances, the MHP was chosen as the baseline solution for the DTC's thermal management of the components.

REQUIREMENTS & TRADE-OFF

System requirements were specified including as a minimum, a noise budget compatible with 6.25 Gbps HSSL, technological characteristics of the system, thermal and mechanical requirements as presented in the following table.

Table 1. Requirements

Designation	Criteria
Data rate	6.25 Gbps
Noise Budget	Differential Return loss : S11 < -25 dB + freq [GHz] from 1 MHz to 12 GHz Differential insertion loss : S21 < -0.5 dB @ F= 5GHz Crosstalk: S31&S41 < -30 dB from 1 MHz to 12 GHz
Minimum number of LGA pads	800 minimum
Number of package I/Os for die	1000 minimum
Pitch	1 mm
Housing Material	Space qualified material (outgassing = as RML <1% and CVCM < 0,1%)
Contact Interfaces	Gold
PCB compatibility	High frequency material
Mass	<CCGA solder assembly solution <20 gr for the electrical interposer
Thermal impedance reduction	50%
Thermal impedance	Compatible with a heat extraction system placed on the top of the package. The TIM window should be as a minimum 30 mm x 30 mm.
Dissipated power	15 W nominal
Reliability	Vibration + 1500 thermal -55/ 125°C
Country	Develop and manufacture in a Country without any exportation license

Starting with these requirements, a trad-off was carried out for the different interposer solutions using following criteria: Country (US origin are proscribed), high Speed LGA capability , thickness, pitch (1 mm), reliability and maturity, electrical and mechanical properties, outgassing properties.
From this analyse, the Smiths Interconnect- Hypertac interposer enclosing contacts based on spring technology was selected. Two types of contacts were firstly chosen as shown on the Fig 1 below.

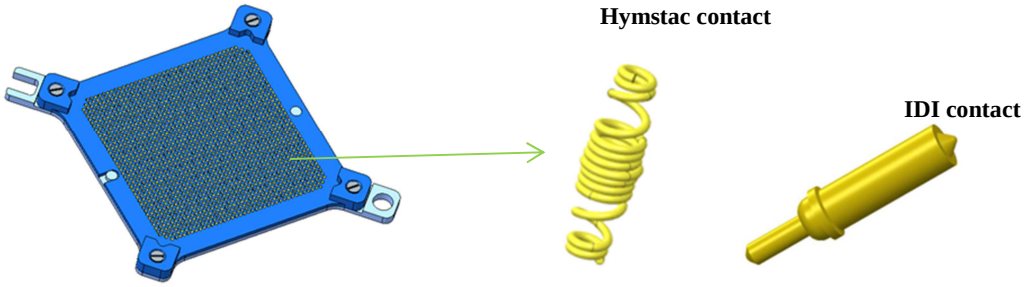

Fig. 1 : interposer overview and type of contacts

DEFINITION AND DESIGN OF THE INTERPOSER SYSTEM

The 1752 contacts interposer has been defined to connect electrically the LGA and the PCB. The mechanical system based on a frame and a stiffener has been developed in order to ensure a good alignment between LGA and the interposer and between the interposer and PCB and at the same time to guarantying application of a holding force able to withstand environment requirement (vibrations and thermal-cycling).
The whole assembly system is presented hereafter.

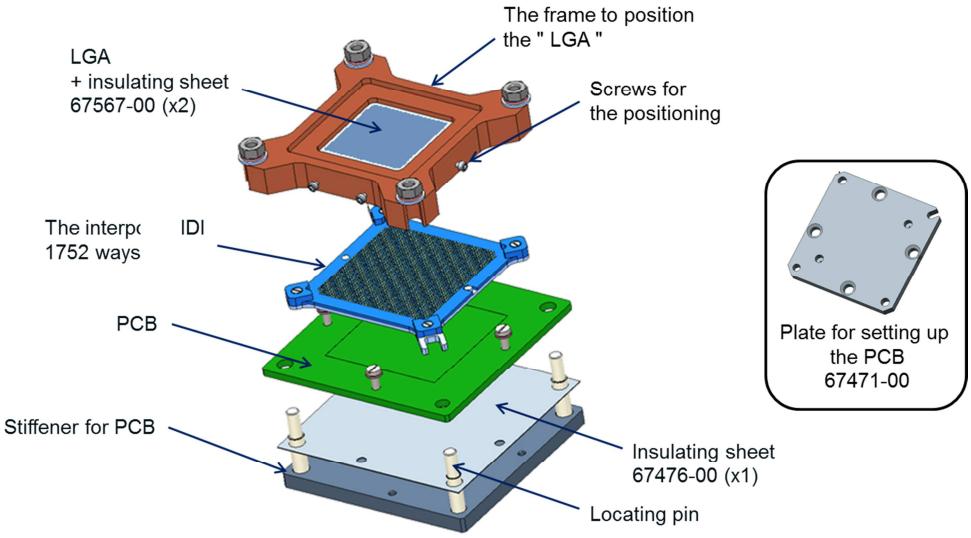

Fig. 2 : Assembly over view

The mechanical behavior of the system and the mechanical parts (frame, stiffener) were independently modeled by Smith interconnects. Using a finite element analysis (FEA) tool the displacement and the stress implied by the compression of the 1752 contacts inside the interposer was evaluated. The Von Mises stress and the deformation of the frame and stiffener were evaluated with the ANSYS tool. The modeling was done with the two types of contacts: IDI contact and Hymstac contact and with different shapes of frame and stiffener. According to simulation results, the solution with IDI contact and star shape frame offer the best solution. However, this assembly (star shape stiffener, and frame using aluminum alloy) is 25% heavier tha the target.
Subsquently, high frequency simulations were done with CST Simulation for the two types of contact and with the characteristics of two kinds of raw materials for interposer: PEEK, and PAI. Results indicate that the solution able to reach TAS requirements in terms of high speed performance is the IDI contact with PEEK material for the interposer.

Measurement have been performed on IDI contacts demonstrating that differential insertion loss and crosstalk were compliant with the requirements.
Finally, the Smiths Interconnect-Hypertac interposer with 1752 IDI contacts and star shape stiffener has been selected for testing.

ASSEMBLY & TEST CAMPAIGNS

For the test campaigns, nine LGA were mounted using the holding system and the Smiths Interconnect-Hypertac interposer on four PCB. The mounting process was easy and fast to realize in spite of many assembling steps. An assembling procedure was written to describe all the steps of assembly.

Fig. 3. Pictures of the Test vehicles

A test plan was established and conducted by Thales Alenia Space. The overview of the test campaigns is shown Fig4. Initial electrical performance tests were performed on all test vehicles and consists in Time domain reflectivity, Eye diagram, Electrical continuity measurements.

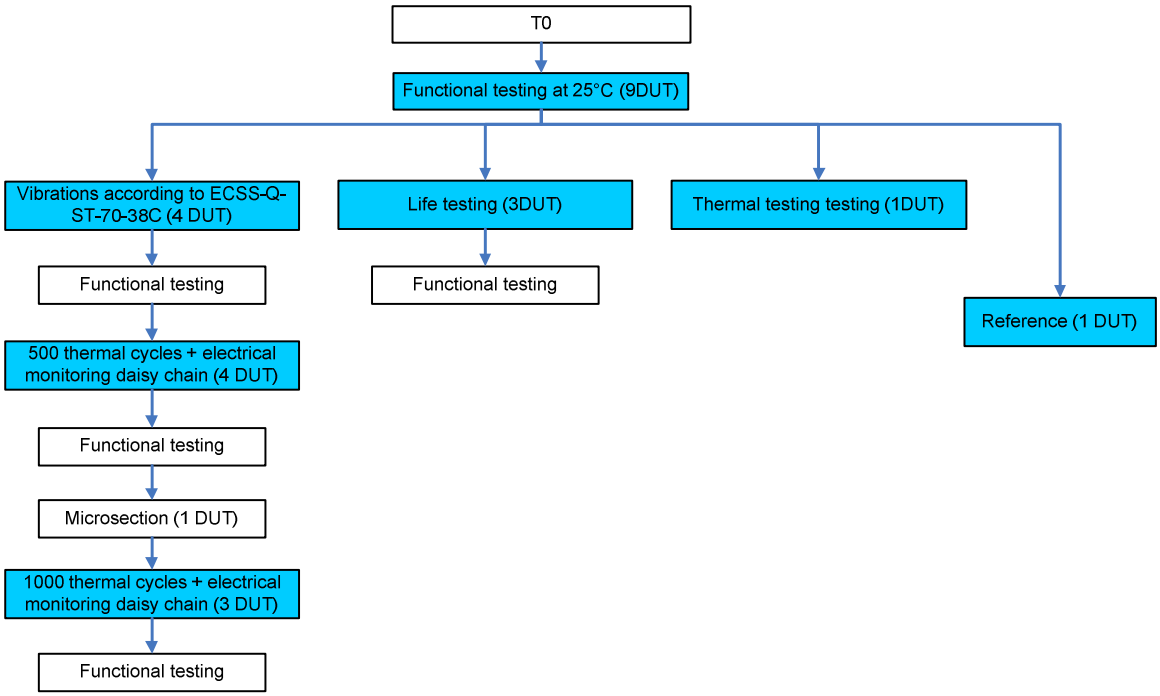

Fig. 4. Synoptic of the test campaigns

TEST RESULTS AFTER ASSEMBLY

Initial electrical performance of the nine DUT were measured: Time Domain Reflectometry (TDR) on High Speed Signal HF1/ HF2/ PHF and Eye diagram of HF2.
Fig 5. presents the routing overview of HF1 with50 Ω impedance lines close to the die edge, 5 lands/line (3 dedicated to GND and 2 for signal In & Out (GSG configuration) and HSSL/LVDS HF2 with 100 Ω impedance differential pair lines. Fig 6 shows routing overview5 of PHF with 50Ω impedance line across the package.

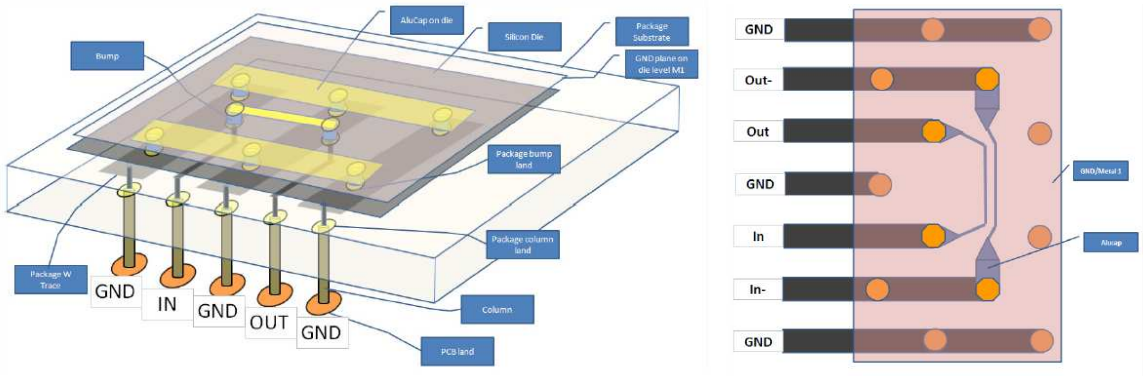

Fig. 5 : HF1 (left) and HF2 (right) routing overview

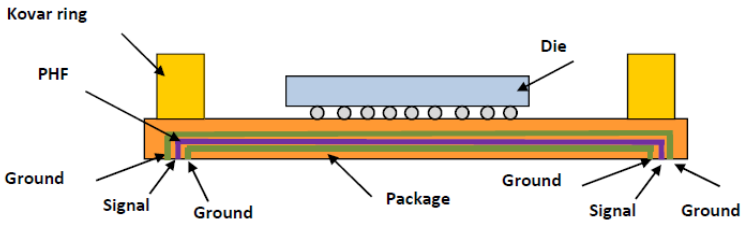

Fig. 6 : PHF routing overview

The initial values were compliant to specification. The daisy chain (DC) resistance was measured and kept as reference.

Environmental Test

The 1500 thermal-cycles were carried out with continuous electrical monitoring of the DC on 4 LGA. Any loss of DC continuity was measured.
After vibration, 500 thermal-cycles, and 1500 thermal-cycles, TDR on HF1 was measured and the values were within the specification. The DC resistance was measured far better the acceptable limit.

After life test, the DC resistance was measured on three LGA. A slight variation was observed, within the acceptable limit. TDR on HF1 was measured and the results indicate a performance compliant to specification.

Thermal test:

Measured and predicted temperatures were within the specifications for ambient and hot cases. Thermal tests have demonstrated thermal efficiently of the proposed thermal management system.

CONCLUSION

The trade-off on solderless assembly on HDI PCB and results from mechanical and electrical simulations have led to the developpement of a solution with Smiths Interconnect-Hypertac Interposer and Smiths Interconnect-IDI contact. The assembly was evaluated in term of electrical performance and resistance under harsh environment (vibration, thermal-cycling, life testing). The thermal management of the system was also assessed through thermal test. Results have highlighted that electrical and thermal performance were within the specification and the system has demonstrated a high reliability under space environment.

This electrical interposer and its mounting system is thus a reliable solderless solution to assemble high pin count packages (1752 I/Os) with high frequency interfaces.

This work has been funded thanks to ESA ARTES program supported by CNES and has been done in response to the ESA ITT AO/1-7693/13/NL/NR – Packaging for Highly dissipating dies on PCBs.