PASSIVE COMPONENT EMBEDDING IN PRINTED CIRCUIT BOARDS FOR SPACE APPLICATIONS

2ND SPACE PASSIVE COMPONENT DAYS (SPCD), INTERNATIONAL SYMPOSIUM, 12-14 OCTOBER 2016, ESA/ESTEC, NOORDWIJK, NL

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PROJECT GOAL

Investigate the suitability of embedding passive components in printed circuit boards for space applications

▸ Overview of available technologies for component embedding
▸ Assessment of the AT&S ECP® technology
▸ Evaluation of reliability of passive component embedding
▸ Realization of a functional demonstrator
▸ Procedures for procurement and qualification of PCBs with embedded components for space applications
Component embedding vs surface mounting

- Reduced volume and weight
- Increased electrical performance
- Larger design freedom
- Elimination of solder joints
- Better mechanical protection
- Lower board complexity = higher yield

- Additional design effort
- Longer time to market due to prototyping requirements
- Impossibility of rework or repair
- Reduction in yield and throughput of the printed circuit board with embedded components
- No existing qualification and procurement procedures
Passive component embedding technology overview

▸ Creating passive components in-situ: “formed passives”
  - Printed thick film technology (Ụ cost, manufacturability; ♂ tolerances)
  - Resistive and capacitive laminates (Ụ performance; ♂ values, design)

▸ Embedding discrete passives into PCB: “placed passives”
  - (Ụ miniaturization, values, performance; ♂ complex process)
EMBEDDED COMPONENT PACKAGING TECHNOLOGY

ECP® Technology
Embedded Component Packaging

Component are embedded inside an organic substrate / PCB core by combination of:
- Component Assembly
- Component Packaging
- PCB Manufacturing

▸ Embedding of both active and passive components
▸ Embedded core can be integrated in various PCB build-ups
▸ Component thickness and pad metallization to be adapted
EMBEDDED COMPONENT PACKAGING TECHNOLOGY
### Available components for embedding

#### Resistors (Panasonic, KOA Speer)

<table>
<thead>
<tr>
<th>Size</th>
<th>Voltage (V)</th>
<th>Power (W)</th>
<th>Tolerance</th>
<th>Operating temperature</th>
<th>TCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>01005</td>
<td>??</td>
<td>0.03</td>
<td>1 %, 5 %</td>
<td>-55 °C to 125 °C</td>
<td>200-300 ppm/°C</td>
</tr>
<tr>
<td>0201</td>
<td>25</td>
<td>0.05</td>
<td>1 %, 5 %</td>
<td>-55 °C to 125 °C</td>
<td>200-300 ppm/°C</td>
</tr>
<tr>
<td>0402</td>
<td>50</td>
<td>0.06 – 0.1</td>
<td>1 %, 5 %</td>
<td>-55 °C to 125 °C</td>
<td>100-200 ppm/°C</td>
</tr>
</tbody>
</table>

#### Capacitors (AVX, Murata, TDK)

<table>
<thead>
<tr>
<th>Type</th>
<th>Size</th>
<th>Range</th>
<th>Voltage (V)</th>
<th>Tolerance</th>
<th>Thickness (µm)</th>
<th>TCC</th>
</tr>
</thead>
<tbody>
<tr>
<td>C0G</td>
<td>0201</td>
<td>1 – 100 pF</td>
<td>10 – 50</td>
<td>5 %</td>
<td>150 – 330</td>
<td>30 ppm/°C</td>
</tr>
<tr>
<td>X5R</td>
<td>0201</td>
<td>0.1 – 10 nF</td>
<td>2.5 – 50</td>
<td>10 – 20 %</td>
<td>110 – 330</td>
<td>±15 %</td>
</tr>
<tr>
<td>X5R</td>
<td>0402</td>
<td>1 – 1000 nF</td>
<td>2.5 – 50</td>
<td>10 – 20 %</td>
<td>110 – 330</td>
<td>±15 %</td>
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<tr>
<td>X7R</td>
<td>0201</td>
<td>0.1 – 10 nF</td>
<td>2.5 – 25</td>
<td>10 %</td>
<td>150 – 330</td>
<td>±15 %</td>
</tr>
<tr>
<td>X7R</td>
<td>0402</td>
<td>1 – 10 nF</td>
<td>6.3 – 25</td>
<td>10 %</td>
<td>150 – 330</td>
<td>±15 %</td>
</tr>
</tbody>
</table>
TEST BOARD

Board Type I

- Board level reliability and component characterization
- Components selection based on availability and BTII
  - 33 Ω, 0402 / 10 kΩ, 0402 / 10 kΩ, 0201 / 1 MΩ, 0201 from Panasonic
  - Murata 10 pF & 100 pF (0201, 150 μm), AVX 10 nF (0402, 300 μm, 16 V to 50 V and 150 μm, 6.3 V) and Murata 100 nF (150 μm, 6.3 V)

- Test structures
  - Probe pad test structure for electrical measurement of components
  - Disk, comb and tree test pattern for interlayer and intralayer insulation
  - Daisy chains (0-ohm resistors) for continuity and interconnect resistance
  - Interconnect stress test (IST) patterns on separate coupon
EVALUATION TEST PLAN

Chart I: INCOMING INSPECTION

- Visual inspection
  - Capacitor
    - El. meas. at room temperature
      - El. meas. at low and high temp.
  - Resistor
    - El. meas. at room temperature
      - El. meas. at low and high temp.
  - Overload
  - Continuity
    - Interconnection resistance
      - Insulation resistance
        - Dielectric withstand voltage

To Chart II

ESCC 3009
ESCC 4001

ECCS-Q-ST-70-10C
ESCC 3009 & 4001

20x BTI + 10x BTI-SM

ECCS-Q-ST-70-10C
EVALUATION TEST PLAN

Chart II: STRESS TESTING

INTERCONNECT LEVEL

BTI1-2

Vibration

Continuity

Interconnection resistance

El. meas. at room temperature

BTI3-4

Mechanical shock

Continuity

Interconnection resistance

El. meas. at room temperature

BTI5-6

Bending

Continuity

Interconnection resistance

El. meas. at room temperature

BTI7-8

Thermal cycling

Continuity

Interconnection resistance

El. meas. at room temperature

COMPONENT LEVEL

BTI9-11

Resistor

To Chart III

Capacitor

BOARD LEVEL

BTI15-16

Thermal stress

Insulation resistance

Dielectric withstanding voltage

BTI17-18

Damp heat

Insulation resistance

Dielectric withstanding voltage

COUPON

IST

Continuity

Interconnection resistance

Continuity

Interconnection resistance

Continuity

Interconnection resistance

Continuity

Interconnection resistance

Continuity

Interconnection resistance

ESCC 3009

ESCC 4001

ECCS-Q-ST-70-38C

AEC-Q200-005

ECCS-Q-ST-70-10C

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EVALUATION TEST PLAN

Chart III: COMPONENT LEVEL

Resistor

BTI9

Power step-stress testing

BTI10-11

Operational life (1000 h)

El. meas. at room temperature

Operational life (1000 h)

El. meas. at room temperature

Capacitor

BTI12

Voltage step-stress testing

BTI13-14

Operational life (1000 h)

El. meas. at room temperature

Operational life (1000 h)

El. meas. at room temperature
<table>
<thead>
<tr>
<th>Test</th>
<th>Type</th>
<th>Resistor</th>
<th>Capacitor</th>
<th>0-ohm resistor</th>
<th>Board</th>
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<td>Overload</td>
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<td>n.a.</td>
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<td>n.a.</td>
<td>n.a.</td>
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<td>n.a.</td>
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<td>Bending (AEC-Q200)</td>
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<td>n.a.</td>
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<tr>
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<td>Surface-mount</td>
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<td></td>
<td>n.a.</td>
<td>n.a.</td>
</tr>
</tbody>
</table>
TEST RESULTS

Component performance

▸ Resistors are within spec for 5 % tolerance, outside spec for 1 % tolerance

▸ Capacitors are within spec for capacitance, loss factor, insulation resistance and voltage proof testing

▸ Resistor operating life time (2000 hours, 70 °C with power cycling)
  - 0402 embedded resistors perform slightly worse than SMT resistors
  - 0201 embedded resistors started failing after 512 hours

▸ Capacitor operating life time (2000 hours, at 85 °C and 2x $V_R$)
  - Decrease in capacitance is larger for the embedded components compared to their surface-mount equivalents
  - X5R capacitors out of spec after 1000 hours of testing

More detailed test results were presented at EMPS-7, Portsmouth, UK, on 13 and 14 April 2016 (http://emps.port.ac.uk/)
Spacecraft Interface Module (SIM)

- Proven flight board developed and tested in-house at QinetiQ Space for various missions (IXV, Proba-2 and Proba-V)
- Redesigned for the use of embedded passives by AT&S
  - Layout and dimensions of the board are not changed
- Twelve layer rigid-flex construction with two embedded cores
Test results

- Initial electrical tests, FPGA tests and functional tests passed
- Performance is on par with the standard SIM-FUMO board, despite non-optimized layout
Embedded component area gain

- 44% of all capacitors and 20% of resistors replaced
  - Smaller size with lower voltage and power rating used
  - Proper redesign would possibly reduce board size by factor of 2
SUMMARY

Status of passive component embedding

▸ Performance of embedding technology is at high level
  - Board Type II performed on par with its SMT counterpart
  - No failure observed in interconnection to component (except for IST)

▸ Embedding has minor impact on components
  - Component performance is adequate, except for 0201 resistors
  - Operating life time does not match space requirements

▸ Available components are limitation for space applications
  - Range of available values is limited, no European supply chain, voltage and temperature ratings not sufficient for derating
  - Qualification testing and lot screening need to be upgraded to ESCC requirements and better matched with embedded technology

▸ General considerations
  - Testing of PCBs with embedded component is challenging
  - No automated design flow for space PCBs with design rule checks
  - No repair possible
ASPIRE
INVENT
ACHIEVE