



Ka-band Surface-Mountable Pseudo-elliptic Filter in Multilayer Micromachined Technology for On-board Communication Systems

P. Farinelli¹, L. Pelliccia¹, B. Margesin², R. Sorrentino³

¹ RF-Microtech, Italy

² FBK – Fondazione Bruno Kessler, Italy

⁴ University of Perugia, Italy



- **Motivation**
- **4th-order Ka-band filter in multilayer micromachined technology**
 - **Design**
 - **Manufacturing**
 - **Experimental results**
- **Conclusions**



Satellite market demands for innovative miniaturized technologies to reduce the dimensions, weight and cost of satellite equipment

Filters, Diplexers (and multiplexer) are key elements in modern multiband and multiservice telecommunications systems

Conventional high Q filters in Ka band and beyond are **based on coaxial TEM mode resonators** allowing for high unloaded Q (>1000). However, they are bulky, heavy in weight and the integration with monolithic circuits is difficult.

Process & RF design definition

Process Definition

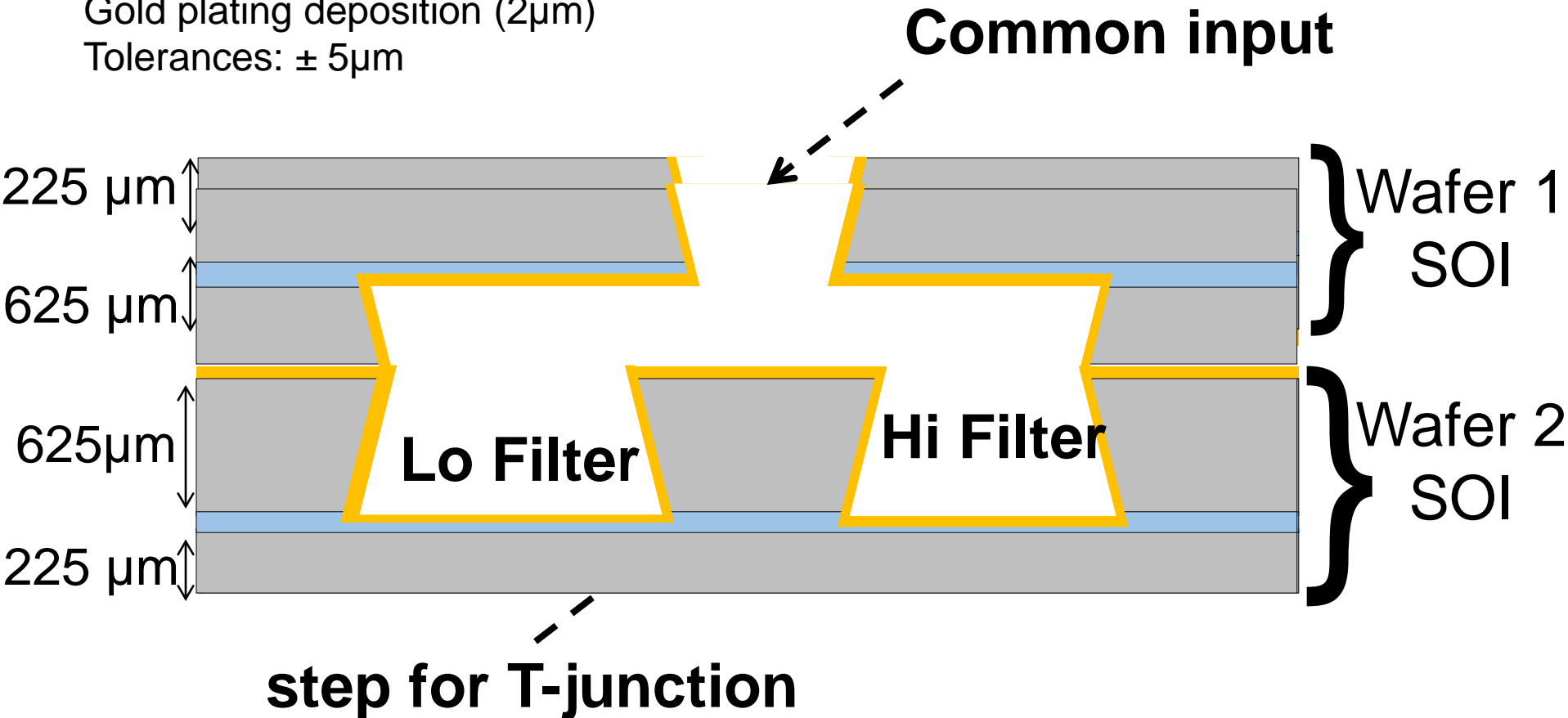
Two Wafer SOI (Silicon On Insulator)

Deep silicon etching

Etching angle: 3 degrees

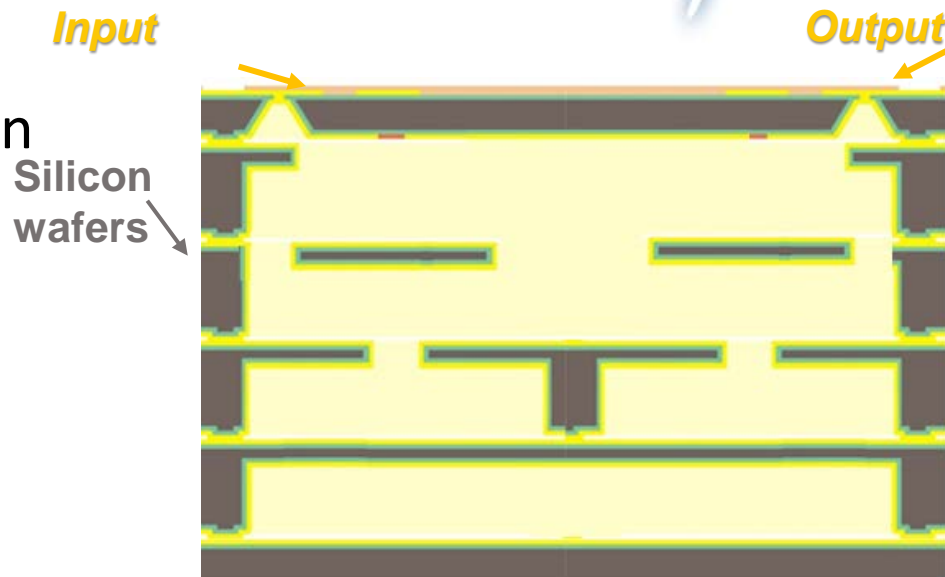
Gold plating deposition ($2\mu\text{m}$)

Tolerances: $\pm 5\mu\text{m}$



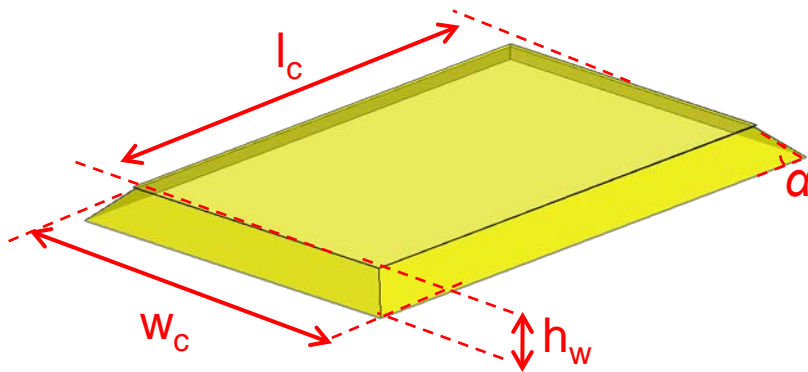
Based on resonant cavities and thin membranes that are:

- **etched** in Silicon/Silicon On Insulator wafers
- **gold-plated**
- **stacked** in multilayer structures



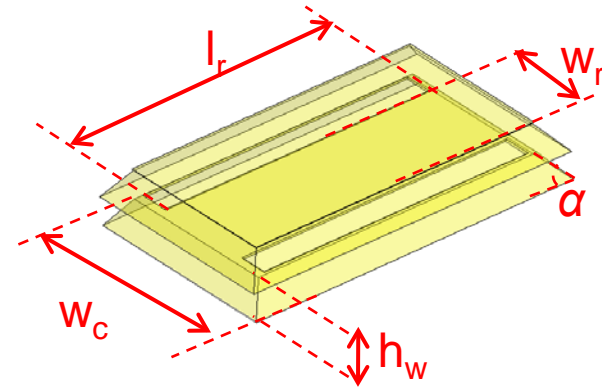
- High miniaturization
- High Q
- Small footprint (multilayer technology)
- Small weight
- High integration (Surface Mountable Devices)
- Low manufacturing tolerances

Micromachined cavities are generally realized as **TE₁₀₁ mode cavities**



TE₁₀₁ mode cavity
Main critical parameters: l_c and w_c

VS



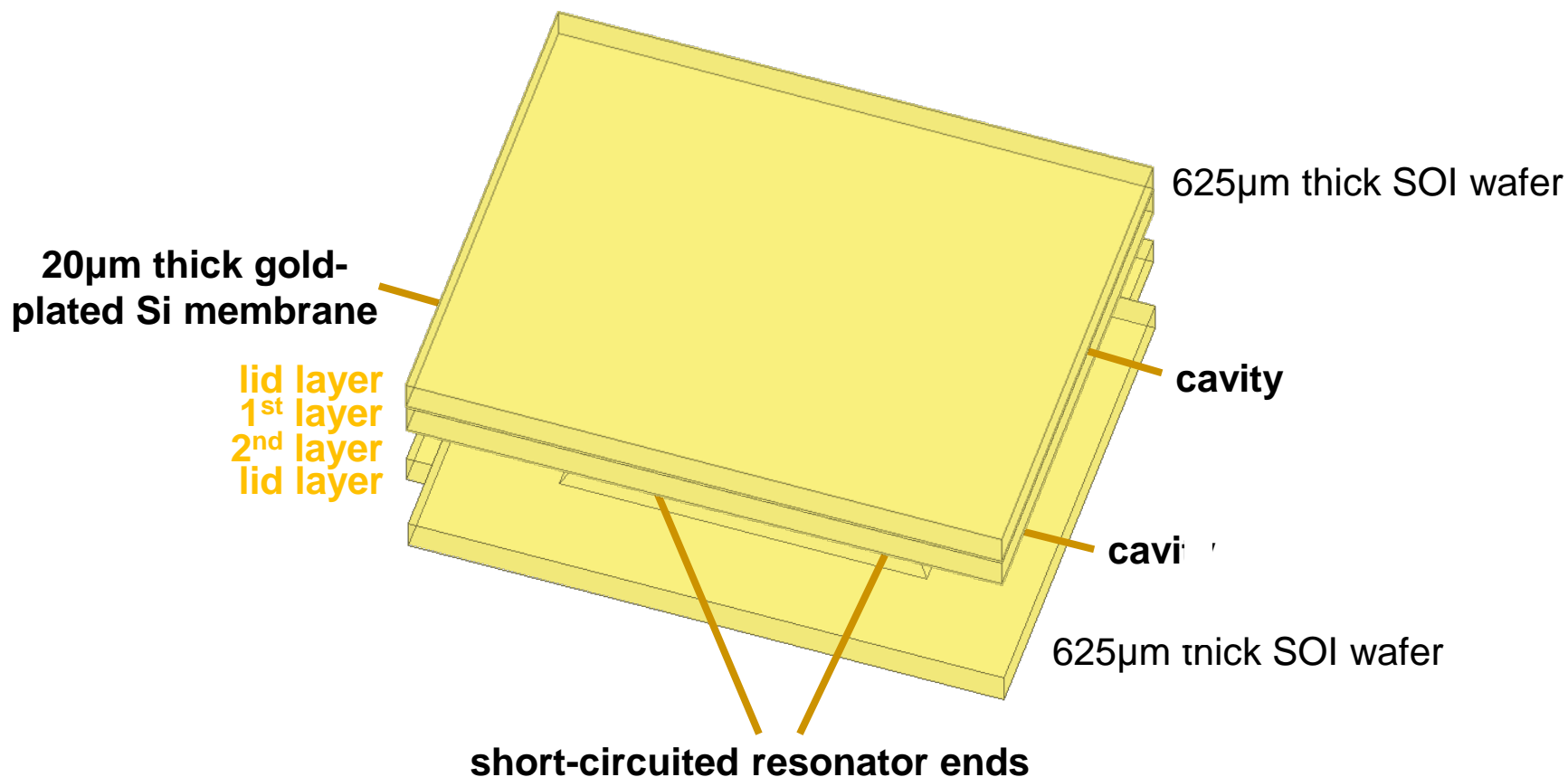
$\lambda/2$ TEM Mode Cavity
Main critical parameter: l_r



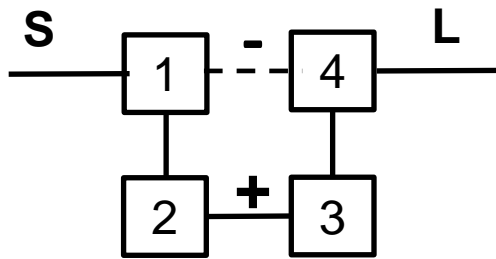
- 1) Number of geometrical parameters affecting the resonant frequency is minimized
- 2) Footprint reduction $\sim 50\%$, Q decrease $< 25\%$

Ka-band $\lambda/2$ TEM Mode Cavity

Resonators are realized as short-circuited membranes etched in the Silicon wafers by Deep Reactive Ione Etching, gold electroplated and stacked by thermo-compressive bonding



4th-order Filter: RF Design



Filter Topology

input/output 50Ω
microstrip feeding
lines

input/output
coupling slots
1st
layer

wings for
capacitive
couplings

2nd
layer

1st res.

4th res.

3rd
layer

square slot

4th
layer

opening for
inductive
couplings

2nd res.

3rd res.

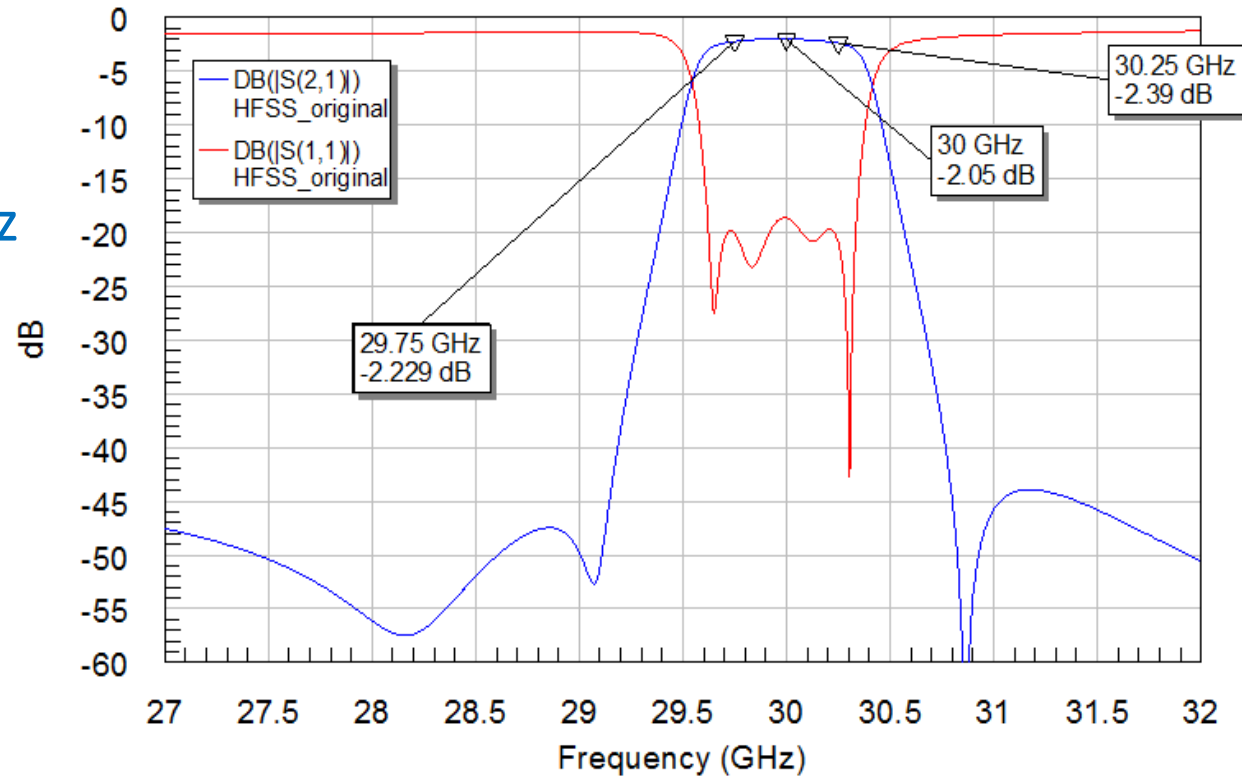
5th
layer

6th
layer

The 4 cavities are placed on 2 levels
→ stacking #6 silicon layers

4th-order Filter: Simulated performance

Centre Frequency: 30GHz
Fract. Bandwidth: 1.8%
Insertion Loss < 2.5 dB
Q ~ 600



Stacking:

- ❑ 1 HR Silicon wafer, 200μm thick (top plate)
- ❑ 4 SOI wafers, 625μm thick each
- ❑ 1 supporting wafer

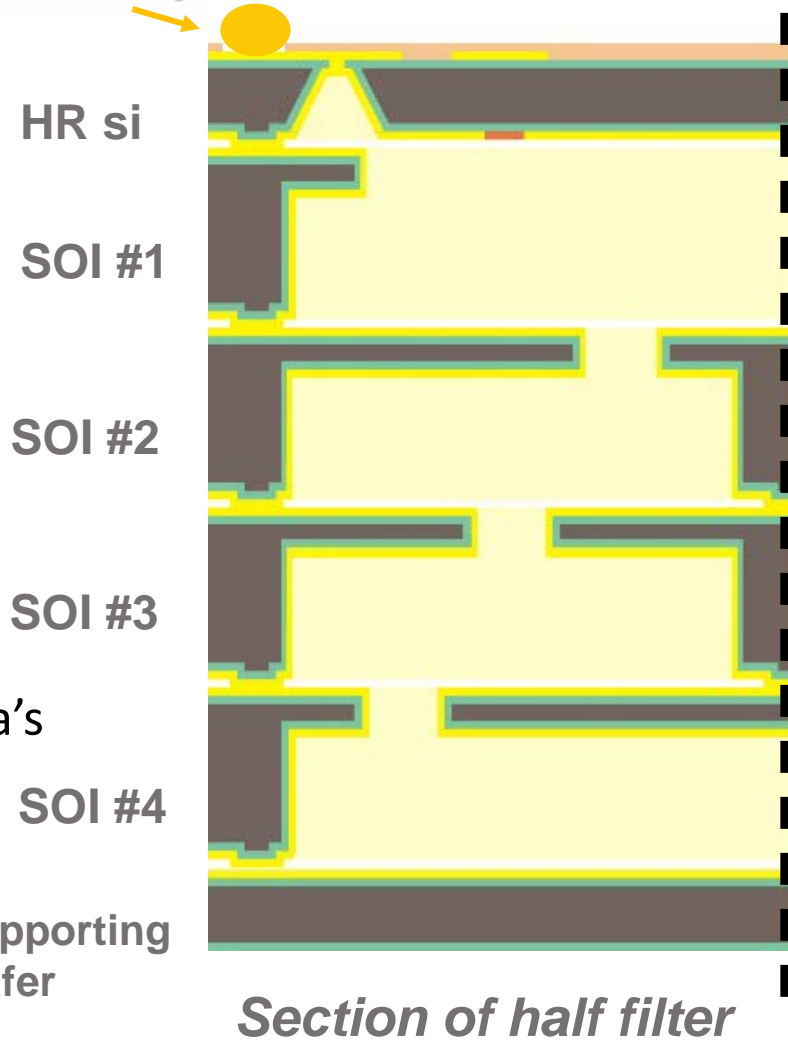
Basic Technological Processes:

- ❑ Deep Reactive Ion Etching (DRIE)
- ❑ Gold Electroplating
- ❑ Anisotropic Etching (TMAH) for Conductive via's
- ❑ Thermo-compressive Wafer Bonding

Manufactured and assembled in FBK - Italy

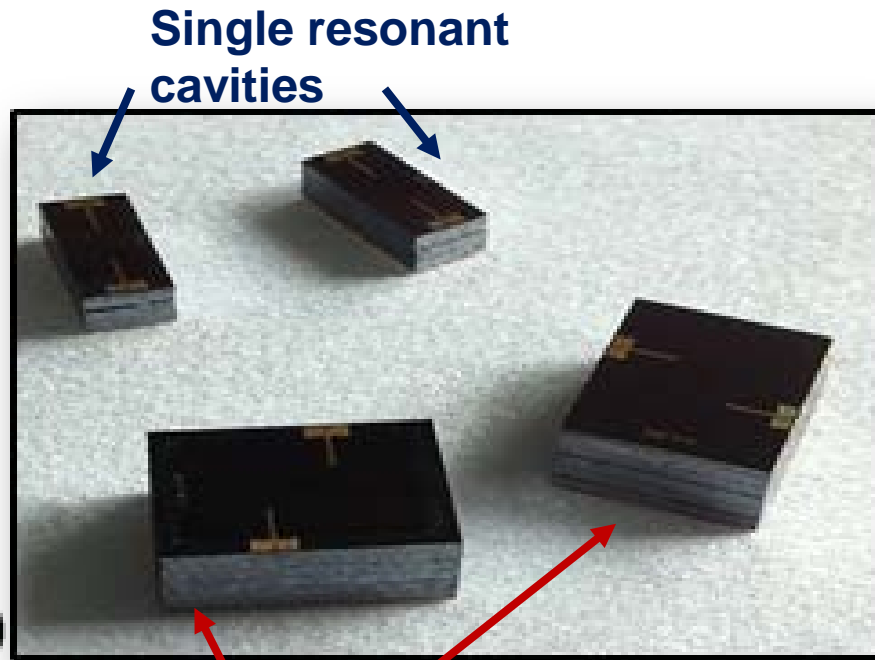


Flip Chip Assembly

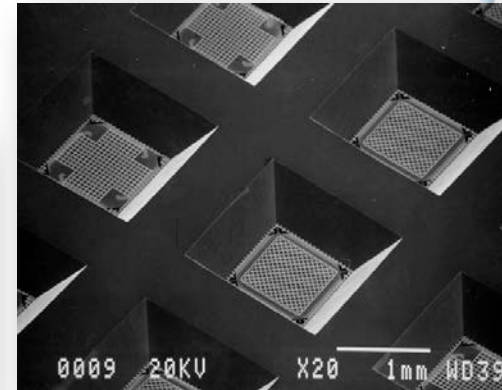


Supporting wafer

Section of half filter



4th order Ka-band Filter



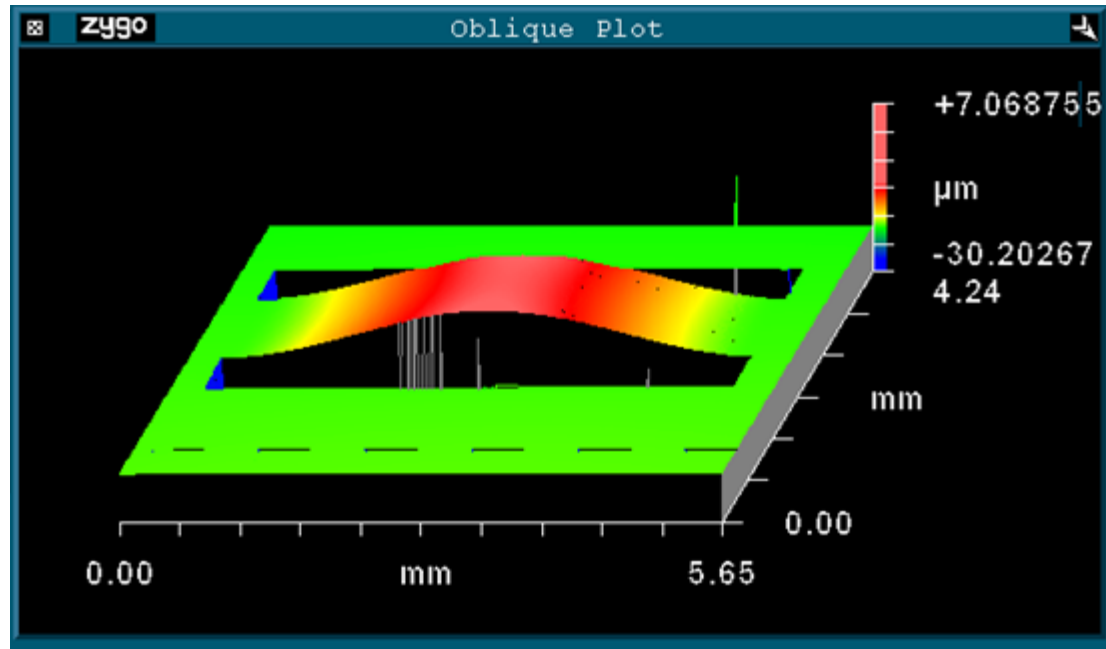
conductive vias



wafer details

Inspections on Membrane flatness *RF μ tech*

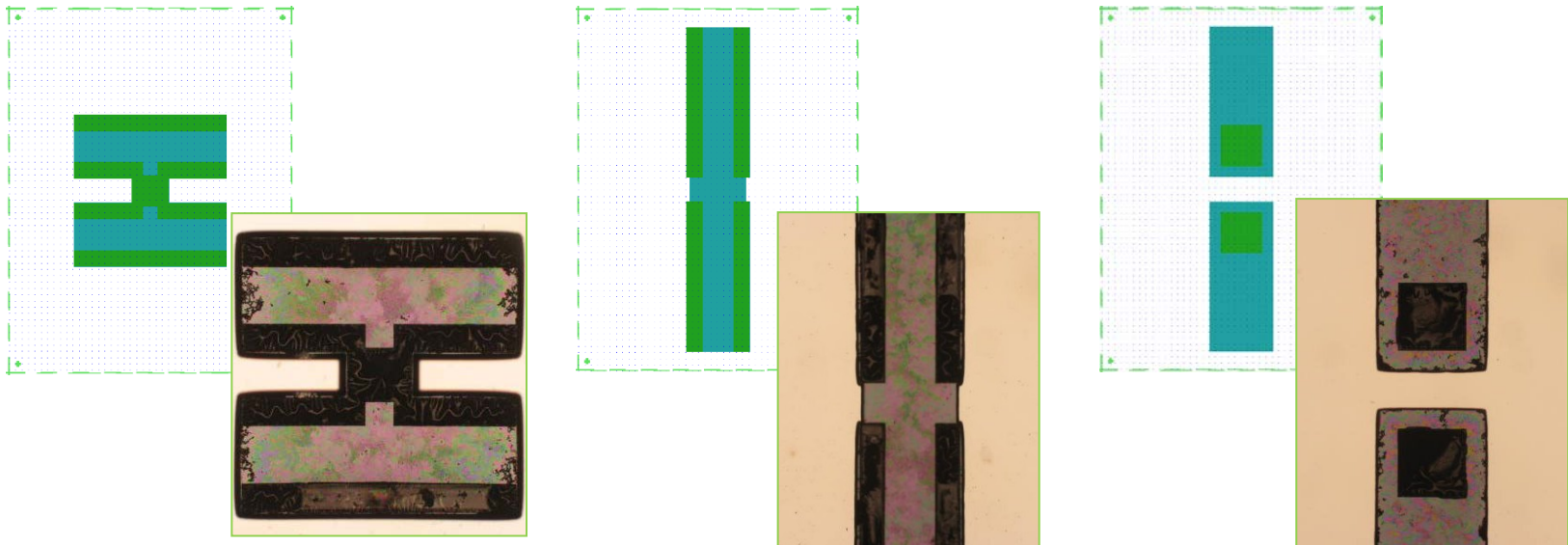
- The final membranes are almost flat (buckling < 3 μ m).



All membranes were longer than designed, because of a non-optimized etching time that caused an over-etching of the cavity side walls (about 60-80 μm for each side). This problem caused:

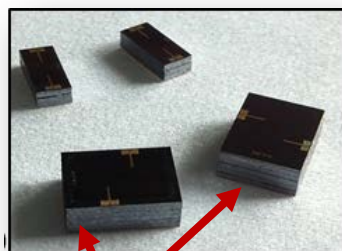
1. longer $\lambda/2$ membranes \rightarrow down-shift of the filter centre frequency (about 600-900 MHz)
2. Larger couplings between cavities that \rightarrow higher RL

In the second run this error will be compensated for by undersizing the masks

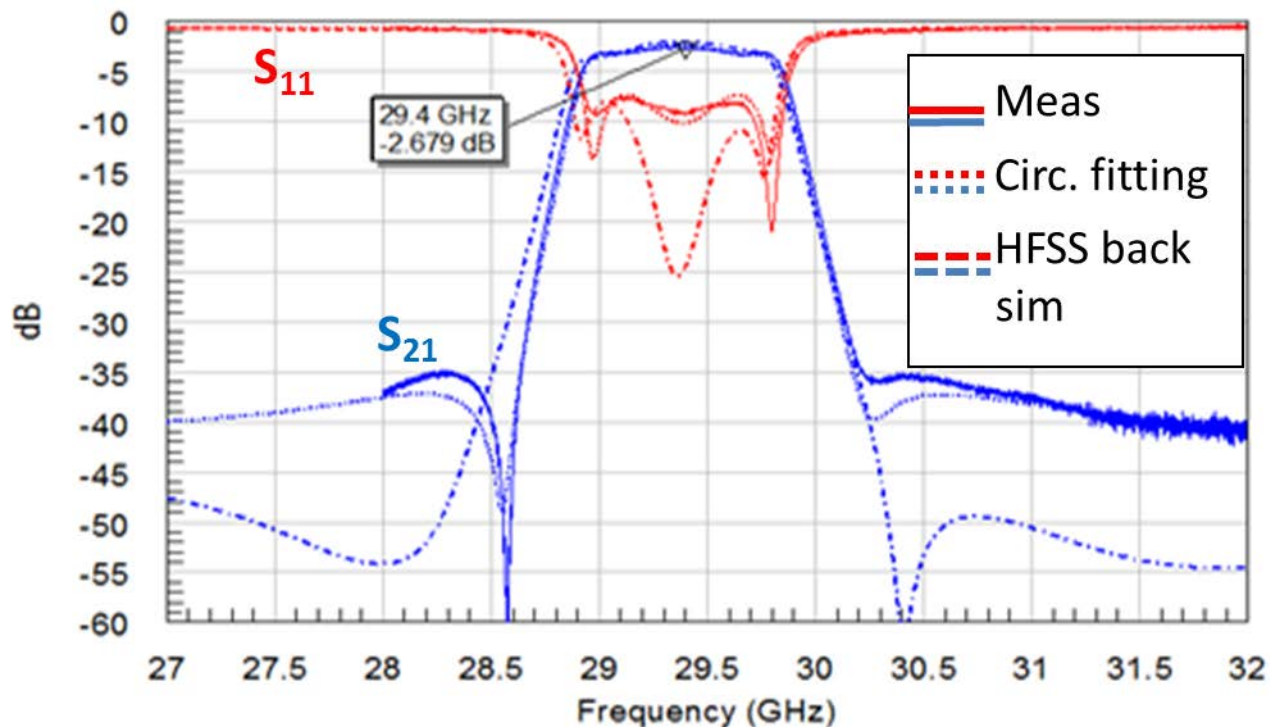


Comparison among measurements, circuital (AWR) and HFSS back simulations, accounting for the actual cavity dimensions

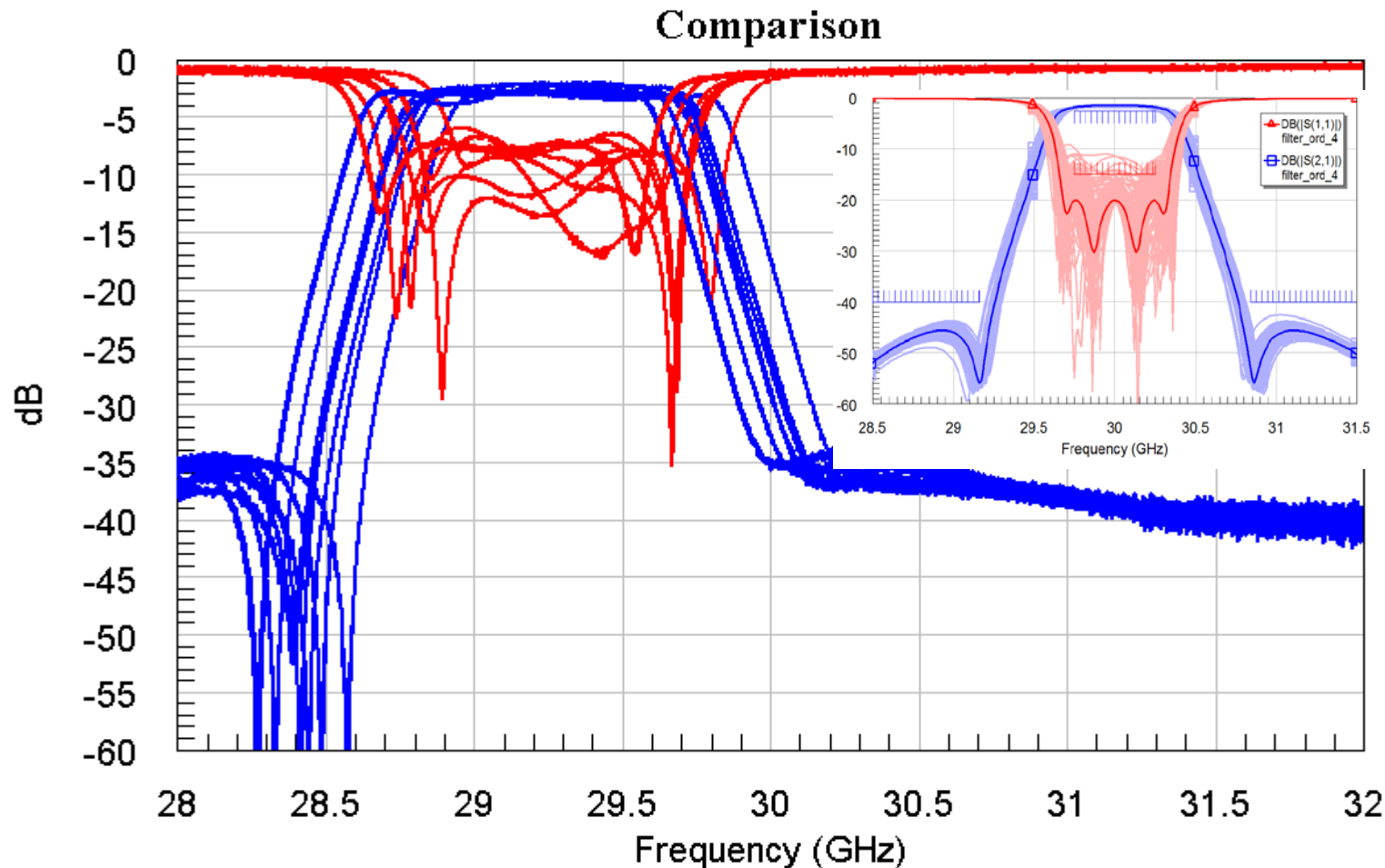
Frequency: 29.4 GHz
Fract. Bandwidth: 2.6'
Insertion Loss < 3 dB
Simulated Q ~ 500



4th order Ka-band Filters



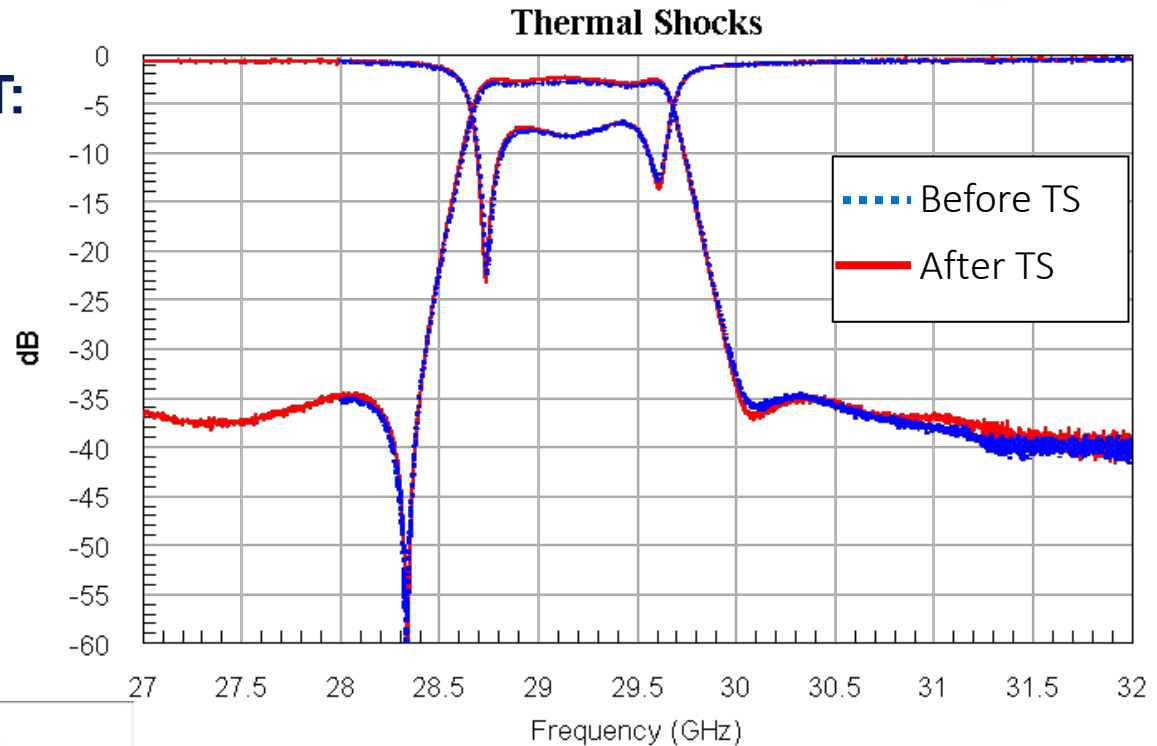
Frequency down-shift by about 600MHz and poor S11 due to the over-etching problem



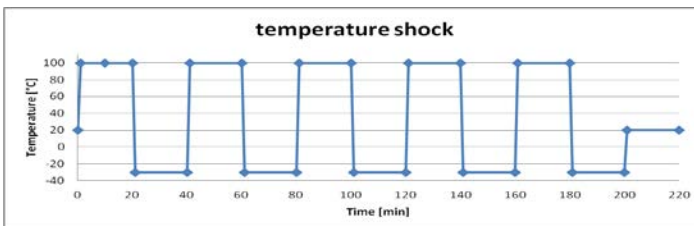
Good agreement between measured performance of #8 samples and Monte Carlo analysis, accounting for manufacturing and assembly tolerances

DEVICES UNDER TEST:
#10 single cavities
#10 4th pole filters

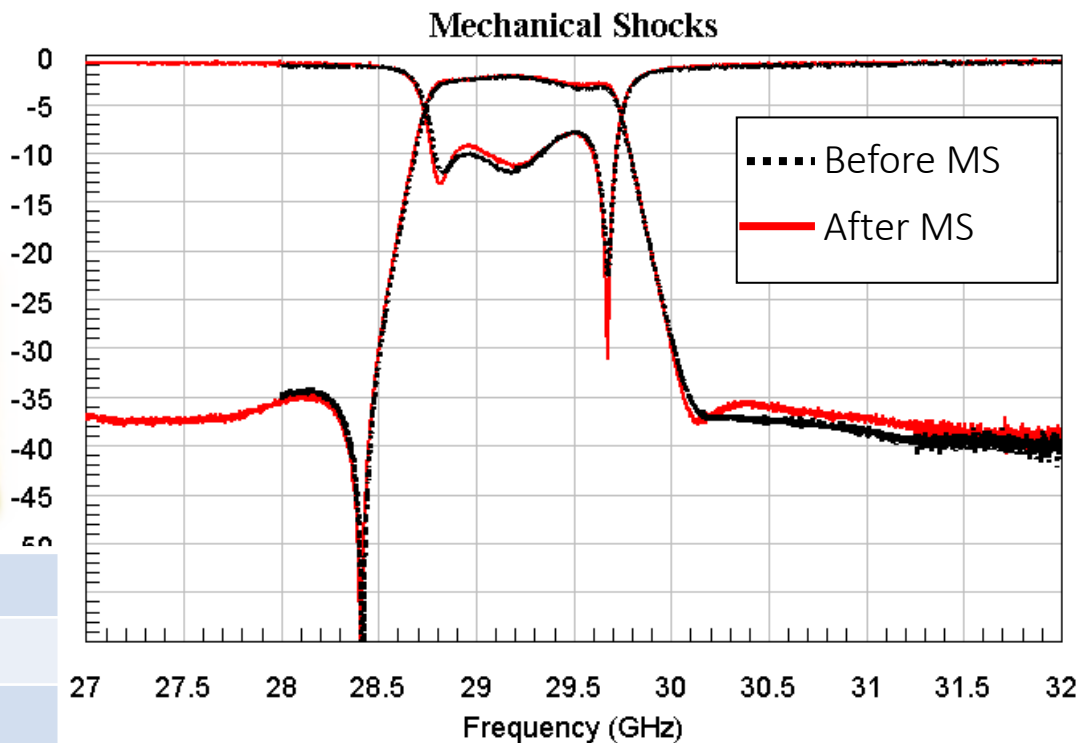
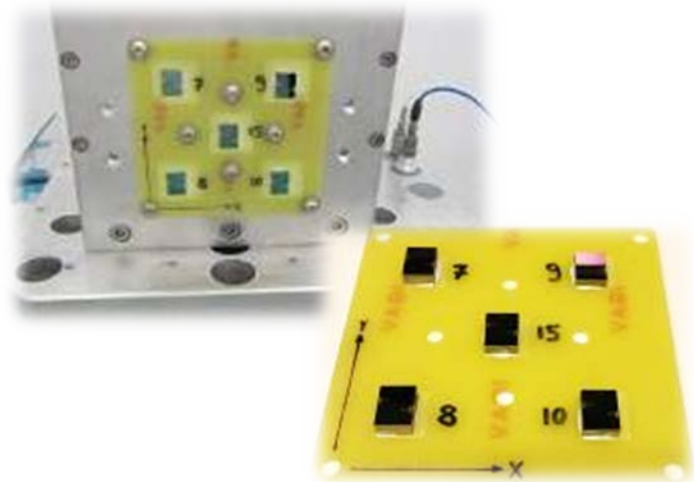
TEST CONDITIONS
#10 cycles -30°/100°
MIL-STD-202G ; Method
107 G ,test condition A-1



**No failure or change in S parameters
for the #20 samples**



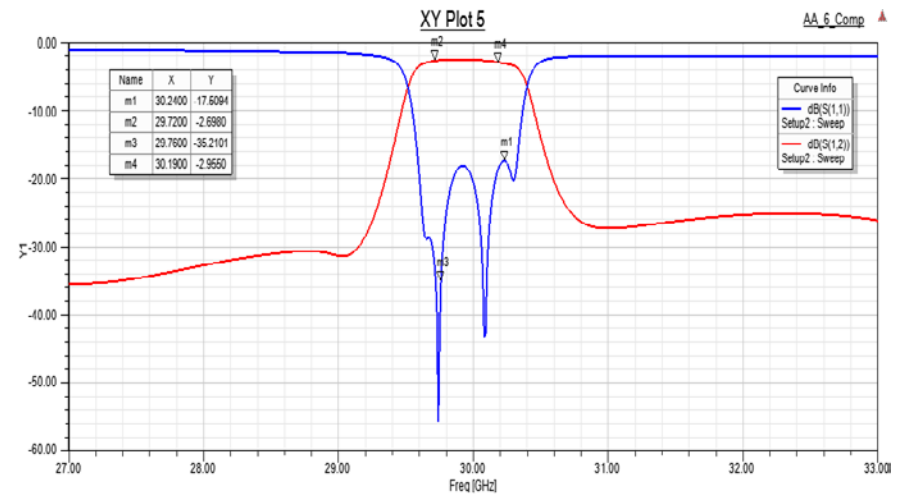
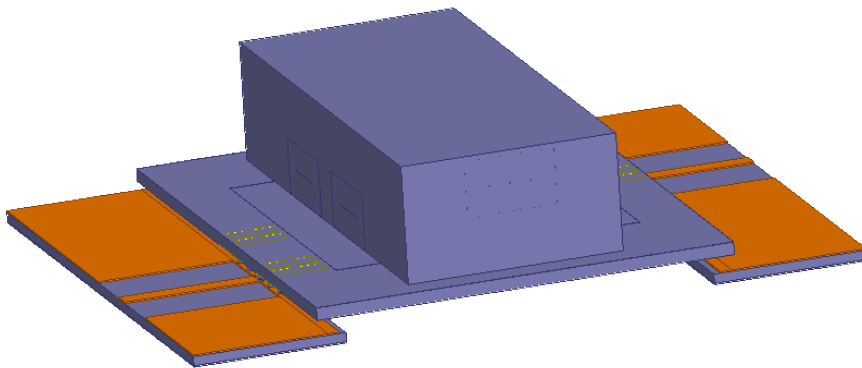
#5 4th order filters were glued on a test board and stressed with mechanical shocks

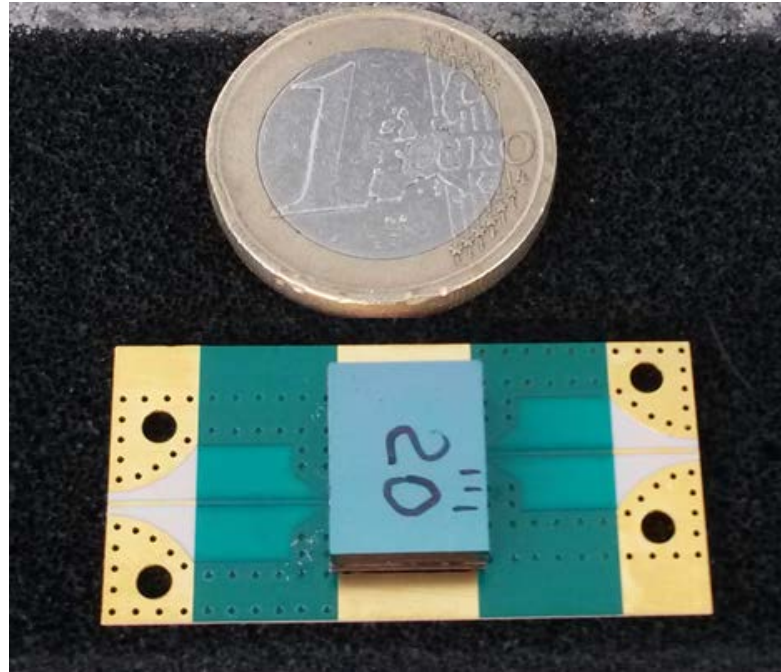


Shape of shock pulse	Half-sine
Peak acceleration	1500 g
Duration of pulse	0.3ms
Number of shocks	9 (3 shocks in each axis)

No failure or change in S parameters for the #5 samples

- The filter will be soldered on a test board to measure the performance of the integrated device.
- The test board has been modeled and designed to ensure good matching and minimize the interconnection loss.





Measurements and thermal shocks are on-going

- A new micromachined resonator has been proposed for Ka–band filters for space applications
- 4th order micromachined surface mountable filters have been designed, fabricated and tested
- Volume occupation is less than 12x9x3mm, weight is 0.75g
- Unloaded Q around 500 and good reproducibility were demonstrated
- Q up to 1000 is expected by increasing the cavity height, i.e. by using thicker wafers
- Good robustness to both thermal and mechanical shocks
- The filter has been integrated in a test board by using standard surface mounting techniques.

ARTES 5.1 project “**MIGNON**”

“**MI**cromachined filters in multi-layer technology for satellite **ON**-board communication systems”

Special thanks to Dr Francois Deborgies and Dr Christoph Ernst from ESA/ESTEC for their support and suggestions.



Thank you for your kind